USER'S MANUAL

PROGRAMMABLE SINGLE-CHIP HIGH-SPEED PULSE GENERATORS

PCL240AS/MS

NIPPON PULSE MOTOR CO., LTD.

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Considerations in Reading this User's Manual

(1) Varied-speed operation means pulse output with S-curve acceleration/deceleration at the start/stop.

(2) Constant-speed operation means pulse output at a constant rate with no acceleration/deceleration.

(3) The input/output logic of each pin indicates the logic under the reset condition.

1. General Description

The PCL240AS and PCL240MS are CMOS LSIs. Each LSI oscillates high-frequency pulses to drive the stepping motor and pulse train input servomotor according to the command written through the CPU bus interface. Thus, using the CMOS LSI, you can perform S-curve acceleration/deceleration, continuous constant-speed control, preset positioning, and origin return.

If you use the PCL-80K, 240K or 240AK, you can replace it with the PCL240AS to enjoy the S-curve acceleration/deceleration function. The PCL240MS can replace the PCL-240MK for the same purpose.

Features

- Motion control made available through S-curve acceleration/deceleration (acceleration and deceleration rates can be independently set)
- Automatic adjustment of maximum speed
- Maximum output frequency of up to 2.4 Mpps
- S-curve acceleration/deceleration made available with the same hardware and software as used for PCL-240AK/240MK
- Interface for servomotor control
- Motion control available with mechanical limit signal input
- Present position counter

2. Specifications

2.1 Specifications

Power Requirement: +5V ±5%

Reference Clock: 4.9152MHz standard (10MHz maximum)

Positioning Pulse Setting Range: 0 to 16,777,215 pulses

Pulse Rate Setting Steps: 1 to 8,191

Pulse Rate Multiplication Setting Range: 0.01 to 300 times (with a reference clock of 4.9152MHz)
0.01 to 81.91 pps with 0.01x
1 to 8,191 pps with 1x
300 to 2,457,300 pps with 300x

Pulse Rate Setting Registers: Three types of FL, FH1 and FH2

Ramping-down Point Setting Range: 0 to 16,777,215

Acceleration/Deceleration Rate Setting Range: 1 to 65,535 (can be independently set)

Up/Down Counter Counting Range: 0 to 16,777,215

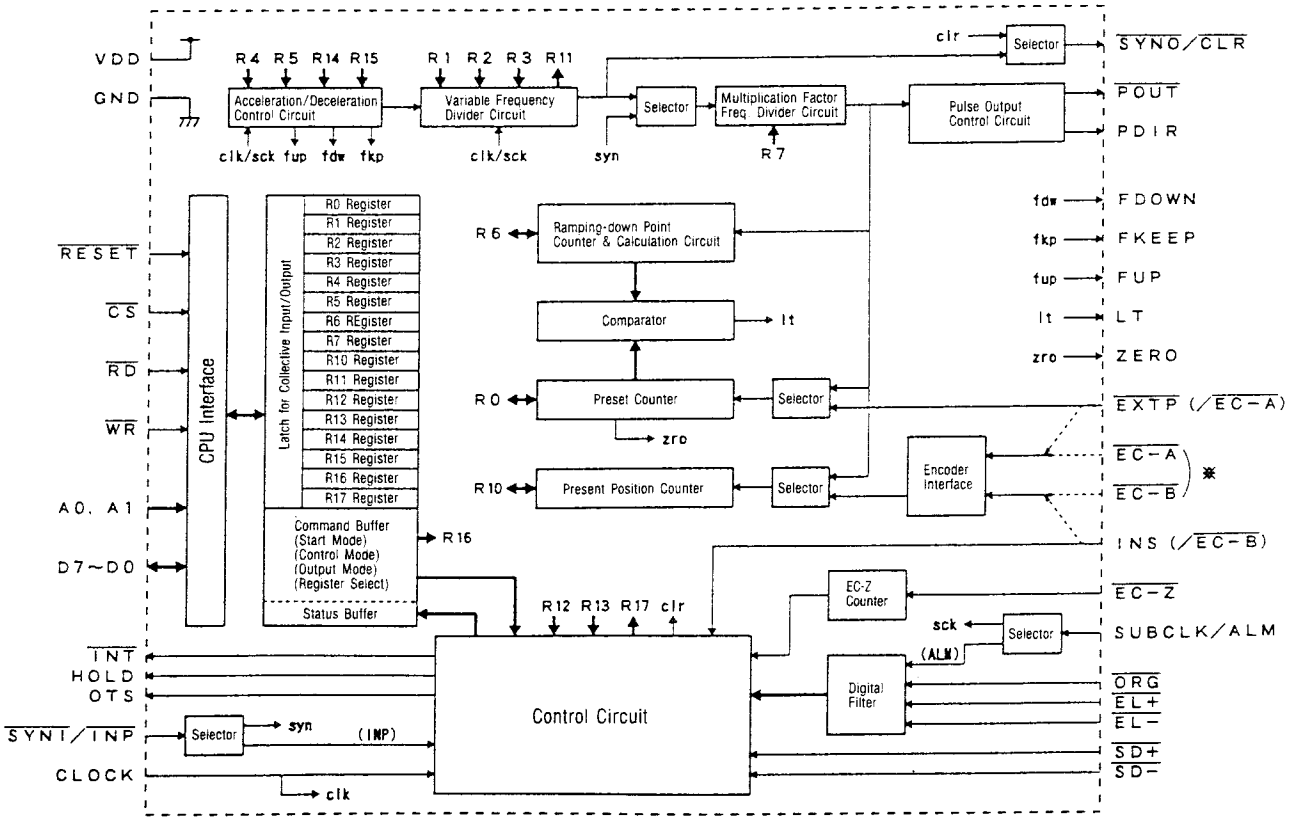
Major Operations Available:
- Constant-speed or varied-speed operation in continuous mode or preset mode
- Constant-speed or varied-speed origin return
- Speed change on the way of operation
- Immediate stop/deceleration-stop
- Timer mode operation

Operating Temperature Range: 0 to +70°C

Storage Temperature Range: −40 to +125°C

Package: PCL240AS: 40-pin DIP
PCL240MS: 44-pin QFP

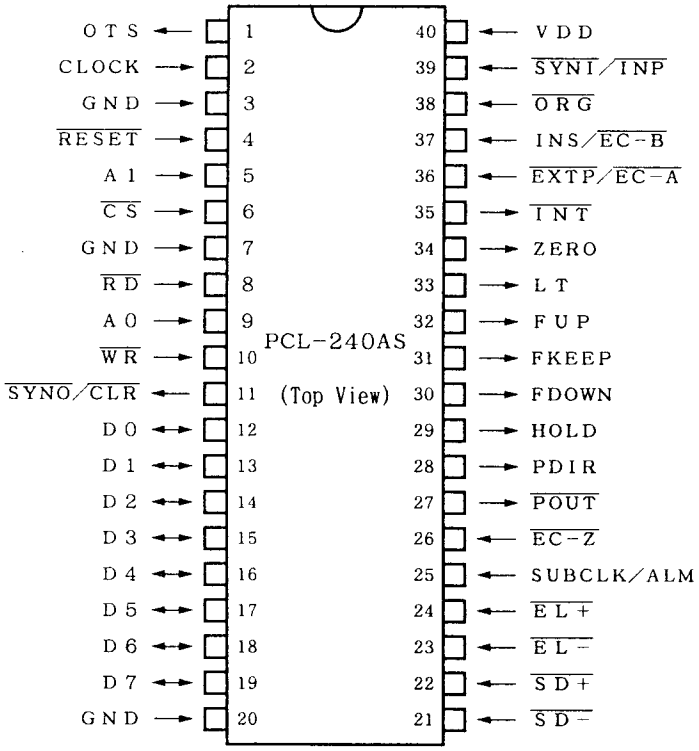
2.2 Block Diagram



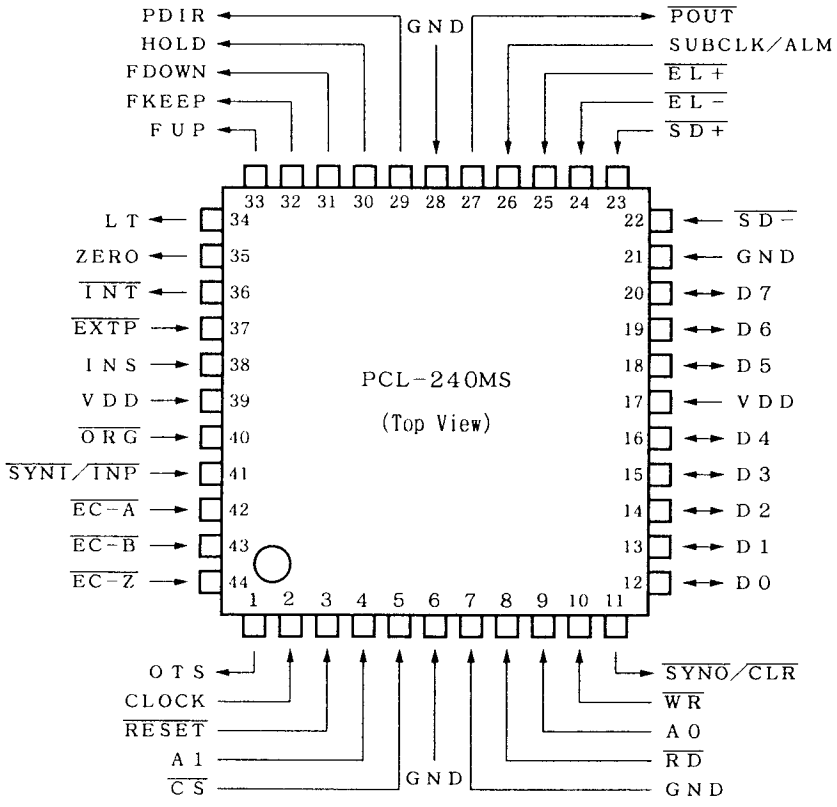
Note: EC-A and EC-B pins are provided for PCL240MS only. With the PCL240AS, EXTP and INS pins are used in common with EC-A and EC-B pins.

2.3 Terminal Pin Layout

PCL240AS



PCL240MS



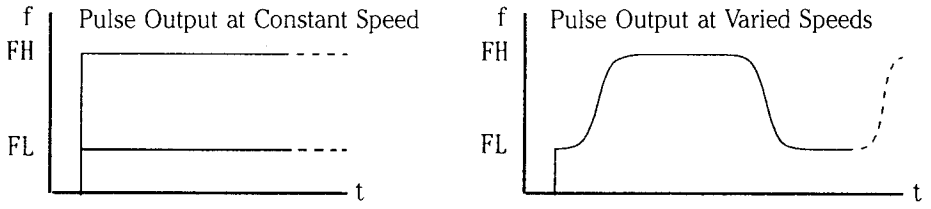
3. Outline of Functions

The LSI generates pulses to control the stepping motor or servomotor according to commands sent from the CPU. You can let the LSI control the motor in a desired mode by setting a variety of parameters.

This chapter roughly describes the functions provided by the LSI. For details, refer to the Chapter 5 "Operation."

3.1 Pulse Output Patterns

The LSI allows you to select a pulse output pattern of either constant speed or varied speeds.



3.1.1 Pulse Output at Constant Speed

The LSI generates pulses at a fixed rate to run the motor at a constant speed from the start to end. You can select the pulse rate from those entered in FL (low speed), FH1 (high speed 1) and FH2 (high speed 2) registers.

3.1.2 Pulse Output at Varied Speeds

The LSI start generating pulses at the FL rate and then accelerates the pulse output to the FH rate. It decelerates the pulse output to the FL rate before stop. Acceleration or deceleration is made in S-curve profile where pulses are output at a gentle rate at the start and end of acceleration and deceleration.

3.2 Commands

You can operate the LSI by writing commands from the CPU to the designated addresses (command buffer). There are four basic types of commands and each type is selected with high-place two bits.

3.2.1 Start Mode Command

7	6	5	4	3	2	1	0
0	**0**	n	n	n	n	n	n

The start mode command is to start or to stop the motion of the LSI. The command also allows you to select a pulse rate (FL, FH1 or FH2), an output pattern (constant-speed or varied-speed) and whether or not to output the $\overline{INT}$ (interrupt) signal.

3.2.2 Control Mode Command

7	6	5	4	3	2	1	0
0	**1**	n	n	n	n	n	n

The control mode command allows you to select:

(1) Whether or not to let the $\overline{\text{ORG}}$ signal stop the motion of the LSI

(2) Whether or not to use the $\overline{\text{SD}}$ signal

(3) Whether or not to place the LSI in the preset (positioning) mode

(4) Moving direction, plus or minus

(5) Whether or not to use the automatic ramping-down point setting function. If the function is made valid, the LSI will automatically decelerate pulse output at the ramping-down point in positioning operation.

(6) Whether or not to use the present position counter.

3.2.3 Register Select Command

7	6	5	4	3	2	1	0
1	**0**	n	n	n	n	n	n

The register select command allows you to select a register for writing data to or reading data from the register. The register is kept as selected until the next register select command is written. With this command, you can select:

(1) A desired register

(2) Whether the data are read or written from/to the register by every 8 bits or in a lump (by 24 bits)

(3) Whether or not to use the general-purpose output signal (OTS) pin

3.2.4 Output Mode Command

7	6	5	4	3	2	1	0
1	**1**	n	n	n	n	n	n

The output mode command allows you to set and select the following:

(1) Input sensitivity of $\overline{\text{ORG}}$ and $\overline{\text{EL}}$ signals

(2) Suspension of acceleration/deceleration on the way

(3) Interchangeable mode with the PCL-240K or standard mode*

(4) Input signal to the preset counter (internal or external pulses)

(5) Pulse output mode (common pulse or 2-pulse mode)

(6) Synchronized operation

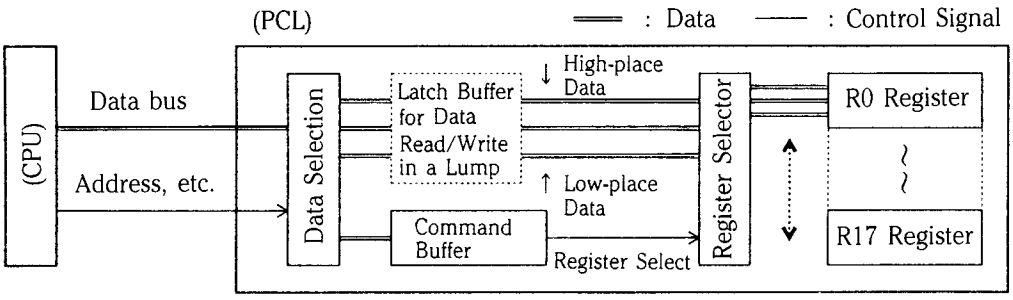
*The PCL240AS and PCL240MS are function-enhanced renewal versions of old model PCL-240K. To make the PCL240AS and PCL240MS compatible with the system built for PCL-240K, they provide the interchangeable mode. Note, however, that if you select the interchangeable mode, enhanced functions such as present position counter, servo control signals ($\overline{\text{INP}}$, $\overline{\text{CLR}}$, ALM), origin return with Z-phase signal, S-curve acceleration/deceleration,

monitoring of command, extension status and registers and collective processing of register data are not available.

3.3 Registers

Registers store numerical parameters (pulse rates, number of output pulses, etc.) and data for extended functions. To read/write data from/to a register, you need to select the register in advance with the register select command. If the interchangeable mode with 240K is selected, you cannot read data from any of registers R1 to R17 and cannot write data in the register in a lump (by 24 bits).

Data Flow from/to Registers



3.3.1 R0 Register, Preset Number of Output Pulses

Enter the total number of output positioning pulses in the R0 register.

3.3.2 R1 Register, FL Pulse Rate

Enter the FL pulse rate in the R1 register. In varied-speed operation, the rate will be used at the start of acceleration and as the target rate for deceleration. Note, however, that the rate is multiplied by the value set in R7 register.

3.3.3 R2 Register, FH1 Pulse Rate

Enter the FH1 pulse rate in the R2 register. In varied-speed operation, the rate will be a target rate for acceleration and be used constantly thereafter until the start of deceleration. Note, however, that the rate is multiplied by the value set in R7 register.

3.3.4 R3 Register, FH2 Pulse Rate

Enter the FH2 pulse rate in the R3 register. The function is the same as the R2 register. Use the start mode command to select either FH1 or FH2 pulse rate.

3.3.5 R4 Register, Acceleration Rate

Enter the acceleration rate in the R4 register. The rate will be used for acceleration in varied-speed operation.

3.3.6 R5 Register, Deceleration Rate

Enter the deceleration rate in the R5 register. The rate will be used for deceleration in varied-speed operation. Note, however, that if the automatic ramping-down point setting function is made valid, deceleration will be made at the rate entered in the R4 register.

3.3.7 R6 Register, Ramping-down Point

Enter the starting point of deceleration in varied-speed or positioning operation in the R6 register. If the automatic ramping-down point setting function is made invalid, enter the number of pulses required for deceleration. If the automatic ramping-down point setting function is made valid, enter 0 or an offset value.

3.3.8 R7 Register, Multiplifcation Factor

Enter in the R7 register the factor to multiply the pulse rates entered in R1, R2 and R3 registers.

The following registers R10 to R17 are effective only with the LSI placed in the standard mode.

3.3.9 R10 Register, Present Position Counter

The LSI has a present position counter (up/down counter for position control). The R10 register allows you to read/write data from/to the counter.

3.3.10 R11 Register, Present Pulse Rate Monitor

This read-only register allows you to monitor the pulse rate at which the LSI is outputting pulses. Note, however, that the rate monitored is the parameter entered in the R1, R2 or R3 register and is not multiplied by the parameter entered in the R7 register.

3.3.11 R12 Register, Extension Mode 1

The R12 register allows you to set details with regard to the present position counter, $\overline{\text{INP}}$ signal, pulse output, $\overline{\text{INT}}$ signal at the ramping-down point, etc.

3.3.12 R13 Register, Extension Mode 2

The R13 register allows you to set details with regard to $\overline{\text{CLR}}$ signal output, ALM signal input, INP signal monitor, origin return with Z-phase signal, $\overline{\text{ORG}}$ signal input, etc.

3.3.13 R14 Register, S-curve Acceleration Section

The R14 register allows you to set the S-curve section at the start and the end of linear acceleration.

3.3.14 R15 Register, S-curve Deceleration Section

The R15 register allows you to set the S-curve section at the start and the end of linear deceleration.

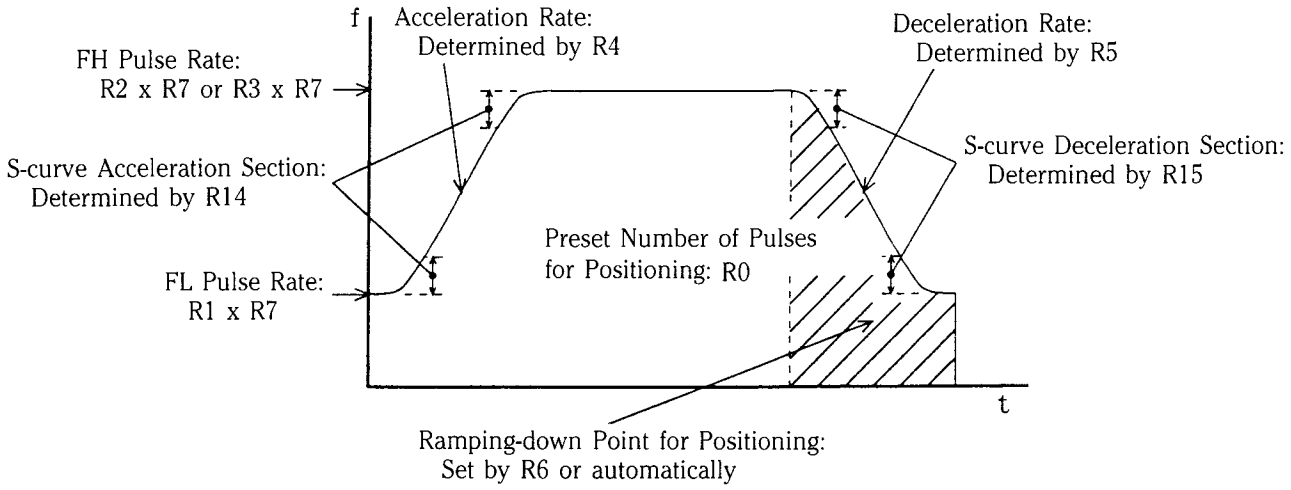
3.3.15 R16 Register, Command Buffer Monitor

The read-only register allows you to monitor the contents written in the command buffer.

3.3.16 R17 Register, Extension Status

This read-only register allows you to monitor the signals, the factor which stopped the LSI from generating pulses and the Z-phase counting.

Register Data Applied Points on Pulse Output Pattern



3.4 Counters

The LSI is equipped with 1) Preset counter for positioning operation, 2) Present position counter which counts output pulses or external pulses, and 3) Ramping-down point counter for automatic deceleration in varied-speed operation.

3.4.1 Preset Counter

Each pulse output lets the preset counter count down the number of pulses entered in the R0 register. In the positioning operation, the LSI stops generating pulses when the preset counter counts down to 0. If you use the same number of pulses, you need to enter the value in the R0 register anew. The present counter counts down even in other than positioning operation. You can check the counter value by reading the R0 register.

3.4.2 Present Position Counter

The present position counter counts output pulses or external signals input through $\overline{\text{EC-A}}$ and $\overline{\text{EC-B}}$ pins.*

If you let it count signals through $\overline{\text{EC-A}}$ and $\overline{\text{EC-B}}$ pins, you can select either 2-pulse signals (plus and minus pulses) or 90° phase-difference signals. In the case of 90° phase-difference signal, you can let it count multiplied signals. You can also select a counting unit in a range of 1/1 to 1/16.

You can check the counter value by reading the R10 register.

*In the case of the PCL240AS which is not equipped with EC-A and EC-B pins, EXTP and INS pins serve in place of them.

3.4.3 Ramping-down Point Counter

Use the ramping-down point counter for automatic deceleration in varied-speed positioning operation. Set the control mode command for use of the automatic ramping-down point setting function, the number of pulses required for deceleration will be calculated and entered in this register during acceleration. The LSI will compare the value with the number of pulses entered in the R0 register. When the preset counter value becomes equal to the value of ramping-down point counter, deceleration will start and the ramping-down point counter will count down. If desired, you can shift the ramping-down point by setting the R6 register.

If the automatic ramping-down point setting function is made invalid, the ramping-down point entered in the R6 register is used for deceleration.

You can check the counter value by reading the R6 register.

3.5 Operation Modes

In combination with the control mode commands, you can operate the LSI in various ways such as positioning and origin return.

3.5.1 Continuous Mode

In the continuous mode, the LSI starts generating pulses upon receiving the start command and continues generating pulses until receiving the stop command.

3.5.2 Origin Return Mode

In the origin return mode, the LSI stops generating pulses upon receiving the $\overline{\text{ORG}}$ signal. Origin return is also available in combination with the Z-phase signal ($\overline{\text{EC-Z}}$).

3.5.3 Preset Mode

In the preset mode, the LSI stops generating pulses upon outputting the total number of pulses entered in the R0 register.

3.5.4 Timer Mode

This mode allows you to use the LSI as a timer. The internal operation is the same as the abovementioned preset mode except for no pulse output in the timer mode.

3.6 Control Functions

The LSI provides sophisticated functions to control the motor in various ways.

3.6.1 Input of External Mechanical Signals

The LSI can input the following signals as position signals from the mechanical system:

(1) Mechanical Limit Signals, $\overline{\text{EL+}}$ and $\overline{\text{EL}-}$

The limit signal in the moving direction immediately stops the LSI from generating pulses. If the limit signal is turned off, the LSI keeps stopping pulse output.

(2) Ramping-down Signals, $\overline{\text{SD+}}$ and $\overline{\text{SD}-}$

In varied-speed operation, the ramping-down signal in the moving direction lets the LSI decelerate the pulse output to the FL pulse rate. When the ramping-down signal is turned off, the pulse output is accelerated to the FH rate.

(3) Origin Signal, $\overline{\text{ORG}}$

In the origin return mode, the origin signal immediately stops the LSI from generating pulses.

3.6.2 Pulse Output Modes

The LSI provides two pulse output modes. In the common pulse mode, it outputs control pulses and direction signals. In the 2-pulse mode, it outputs plus direction pulses and minus direction pulses. You can change the output logic.

3.6.3 Dummy Operation

You can let the LSI perform all activities except for pulse output to check the operation without running the motor.

3.6.4 Servomotor Interface

The LSI provides the following servomotor control signals:

(1) In-position Signal, $\overline{\text{INP}}$

The LSI can input the in-position signal from the servomotor driver. Interrupt signal output is delayed to the input of this signal.

(2) Deviation Counter Clear Signal, $\overline{\text{CLR}}$

The LSI can output this one-shot signal to clear the deviation counter of servomotor driver.

(3) Alarm Signal, ALM

The alarm signal from the servomotor driver stops the LSI from generating pulses.

3.6.5 General-purpose Output Pin

The OTS pin is available to output general-purpose signals.

3.6.6 General-purpose Input Pin

The INS pin is available to input general-purpose signals. In the case of PCL240AS, the INS pin is common to the external input pin, $\overline{\text{EC-B}}$, for the present position counter.

3.6.7 Interrupt Signal Output

Based on two factors, cessation of pulse output and ramping-down point, the LSI can output the $\overline{\text{INT}}$ signal to the CPU.

3.7 Monitor

Through designated addresses, you can monitor the operation status and setting conditions.

3.7.1 Operation Status

You can monitor the following:

(1) Operation status such as cessation of pulse output and deceleration in progress

(2) Input/output signal status

(3) Interrupt factor, cessation factor, etc.

3.7.2 Register Parameters

You can check parameters entered in the registers and values of the counters.

3.8 Basic Operation

The basic operation procedure is as follows:

3.8.1 Writing Commands

Write commands from the CPU to command buffer addresses.

3.8.2 Reading Status

The CPU reads status data from the status addresses (command buffer).

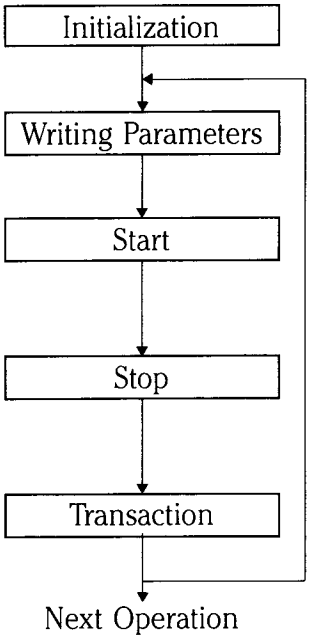
3.8.3 Writing Data to Registers

(1) Using the register select command, select the register to which you want to write data.
(2) Write register data to the addresses for high-place, middle-place and low-place data.

3.8.4 Reading Data from Registers

(1) Using the register select command, select the register from which you want to read data.
(2) The CPU will read register data from the addresses for high-place, middle-place and low-place data.

3.8.5 Typical Operation Flow



Set the pulse output mode, external input signal logic, etc.

Set the number of output pulses, pulse rates, control mode, etc. and write the clear command.

Write the start mode command.

(Read data of position, pulse rate, etc.)

The LSI stops generating pulses with the stop command, upon completion of preset mode operation or with an external signal.

Take appropriate transactions such as reading interrupt factors.

4. Software

4.1 Address Map

Relations of addresses A1, A0, RD, WR and CS with data bus are as follows:

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Description	
L	H	L	L	L	Data bus ⇨ Command buffer	Write
L	H	L	L	H	Data bus ⇨ Low-place register data (bits 7-0)	
L	H	L	H	L	Data bus ⇨ Mid-place register data (bits 15-8)	
L	H	L	H	H	Data bus ⇨ High-place register data(bits 23-16)	
L	L	H	L	L	Data bus ⇦ Status	Read
L	L	H	L	H	Data bus ⇦ Low-place register data (bits 7-0)	
L	L	H	H	L	Data bus ⇦ Mid-place register data (bits 15-8)	
L	L	H	H	H	Data bus ⇦ High-place register data (bits 23-16)	
L	L	L	—	—	Prohibited	
H	—	—	—	—	Data bus = High impedance	

As shown on the table above, A1 and A0 addresses are used as follows:
A1=L and A0=L to write command/to read status
A1=L and A0=H to write/read low-lace register data
A1=H and A0=L to write/read mid-place register data
A1=H and A0=H to write/read high-place register data

4.2 Writing/Reading Data to/from Registers

You need to select the register with the register select command before writing or reading data to/from a register.

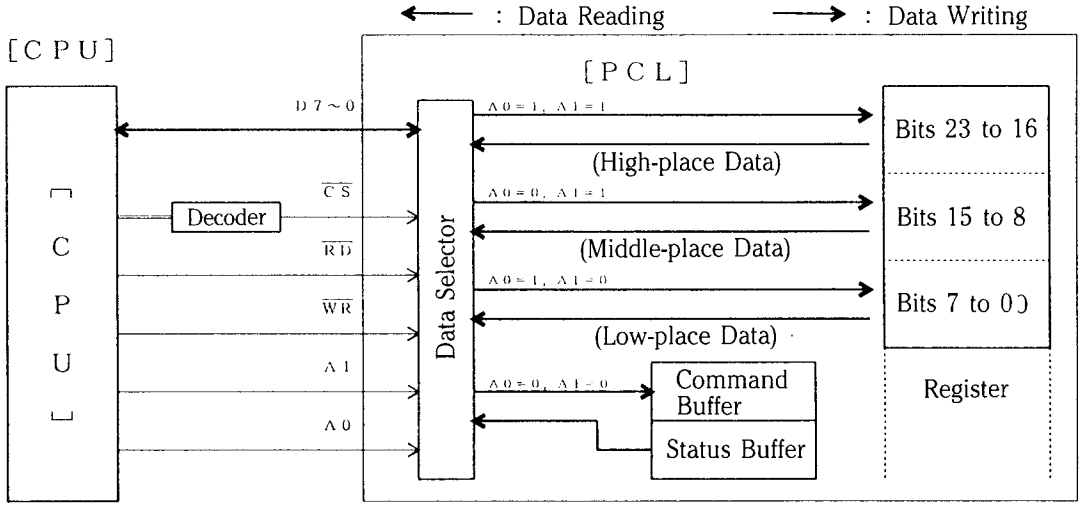
4.2.1 Collective Data Writing and Reading

You can write/read data to/from a register by every 8 bits or by all 24 bits in a lump. You can select either with the register select command. While the LSI is in motion, it is recommended to select the 24-bit collective writing/reading method. Also, note that if the LSI is placed in the interchangeable mode with the 240K, writing or reading data to/from a register is available only by every 8 bits.

Writing/Reading by Every 8 Bits

Data will be written or read from the data bus by every 8 bits to the high-place bits, the middle-place bits and the lower-place bits. Since the write or read timing shifts, if used during pulse output in progress, this method may cause an erroneous writing or reading at the time the counter takes a figure up or down.

Data Flow in Writing/Reading Data by Every 8 Bits



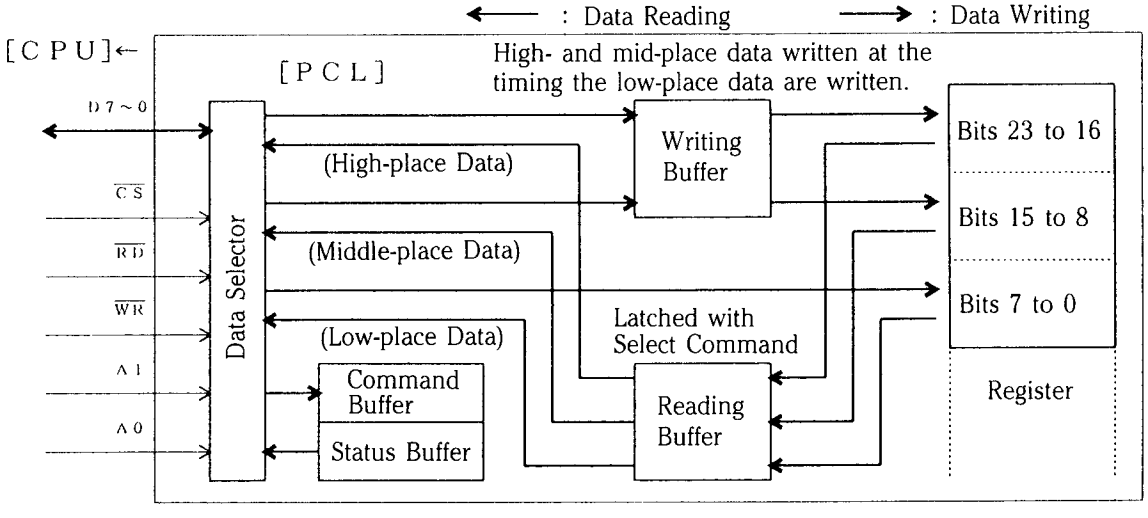
Writing/Reading Data by all 24 Bits in a Lump

When writing, the high- and middle-place register data are once latched in the writing buffer and then are written collectively in the register at the time the low-place register data are written. Be sure to write data in the order of high-place to low-place bits..

When reading, the register data are once copied in the reading buffer at the time the register select command is written and then transferred from the buffer to the CPU.

If the data are collectively written or read during pulse output in progress, counters operate correctly even at the time of taking a figure up or down.

Data Flow in Writing/Reading Data by All 24 Bits in a Lump



4.2.2 Writing Procedure

By Every 8 Bits

(1) Write the register select command (80-95HEX) to the command buffer.
(2) Write data to the high-place address, the middle-place address and the low-place address, individually in a desired order.

By All 24 Bits in a Lump

(1) Write the register select command (A0-B5HEX), which designates the collective write/read method, to the command buffer.
(2) Write all 24-bit data to the high-, middle- and low-place register addresses in that order.
(3) Allow a time length of two cycles of the reference clock (approximately 0.4μs with a reference clock of 4.9152MHz) for internal processing. Do not write any register select command or data during the time.

4.2.3 Reading Procedure

By Every 8 Bits

(1) Write the register select command (80-98HEX) to the command buffer.
(2) Read data from the high-, middle- and low-place addresses, individually in a desired order.

By All 24 Bits in a Lump

(1) Write the register select command (A0-B7HEX), whch designates the collective write/read method, to the command buffer.
(2) Allow a time length of two cycles of the reference clock (approximately 0.4μs with a reference clock of 4.9152MHz) for internal processing. Do not read data during the time.
(Data are copied from the register to the reading buffer.)
(3) Read high-, middle- and low-place data in a desired order.

4.3 Reading Status

You can monitor the present operation status as well as ON/OFF status of $\overline{EL\pm}$, $\overline{ORG}$, ZERO, INS (or $\overline{INP}$), FKEEP and $\overline{INT}$ signals.
If the "By Every 8 Bits" is designated by the register select command, conditions are not latched during processing for reading. If the "Collective Write/Read" is designated by the register select command, conditions at the start of processing for reading are latched. If you need to place the data bus in a stable condition during the read cycle, designate the "Collective Write/Read."

4.4 Reading Extension Status

You can read the extension status from the R17 register. Extension status data you can monitor include the interrupt factor (cessation of pulse output/ramping-down point), pulse output, ON/OFF status of $\overline{SD\pm}$, FUP, FDOWN, LT, ALM and EC-Z. the pulse output suspension factor and the EC-Z counter value.

4.5 Default Conditions

Items	Default (Reset) Conditions
All internal registers	0
Start mode command	00HEX
Control mode command	40HEX
Register select command	80HEX
Output mode command	C0HEX
Pins D0 to D7	High impedance
$\overline{INT}$ pin	High level
$\overline{POUT}$ pin	High level
PDIR pin	High level
HOLD pin	High level
OTS pin	Low level
$\overline{SYNO}/\overline{CLR}$ pin	High level
FDOWN pin	Low level
FKEEP pin	High level
FUP pin	Low level
LT pin	High level
ZERO pin	High level

4.6 Precautions in Designing Software

- To use all functions of the LSI, place it in the standard mode by setting bit 3 of the output mode command at 1. If you place the LSI in the interchangeable mode with the 240K by setting the bit at 0, some functions are not available.
- If you select the "Collective Write/Read" of register data, allow a time length of two cycles of the reference clock between:
  (1) Writing the register select command and reading the data
  (2) Writing the low-place data and writing the next register select command or data.
- Write data to the register in order from the high- to middle- and low-place data if the "Collective Write/Read" is selected.
- Enter 1 or higher value in registers R1 to R3. Enter 2 or higher value in registers R4, R5 and R7. For preset mode operation, enter 1 or higher value in the R0 register.
- Before sending the start mode command, write the clear command (08_{HEX}). The LSI has a latch to keep the stop condition if stopped at the previous stage and you need to reset the latch before starting. The latch can be reset by setting bit 4 of the start mode command at 0.
- Write the start mode command after setting all necessary conditions, since the start mode command starts the LSI generating pulses.
- The register select command does not allow you to read the present conditions. Take care when changing the register select command for interrupt processing.

5. Operation

5.1 Setting Pulse Output Pattern

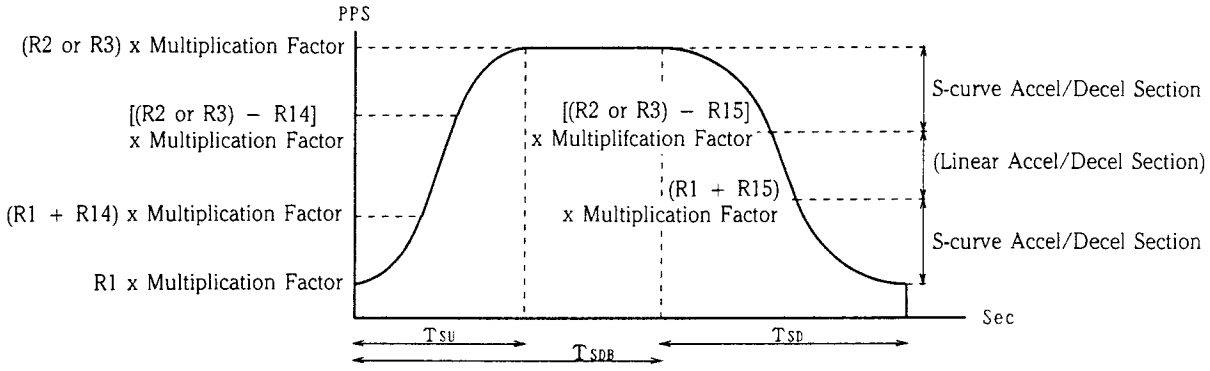
The LSI provides the following two acceleration/deceleration modes:

(1) S-curve acceleration/deceleration with no intermediate linear section
This mode is initiated if registers R14 and R15 are set at "0" or a value higher than "(R2 or R3 value − R1 value) ÷ 2." In this mode the acceleration or deceleration rate is constantly changed from the start to end.

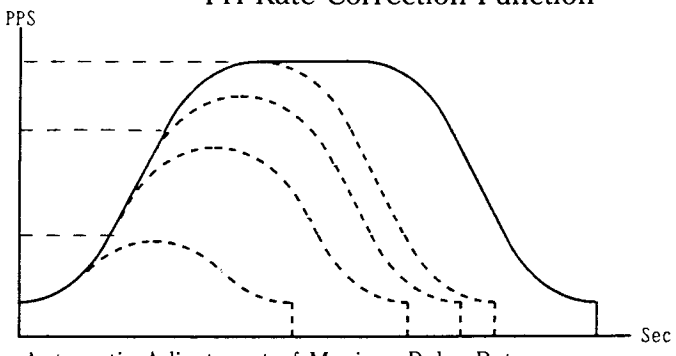
(2) S-curve acceleration/deceleration with intermediate linear section
This mode is initiated if registers R14 and R15 are set at other than "0" and the values are lower than "(R2 or R3 value − R1 value) ÷ 2." In this mode an S-curve acceleration/deceleration is made at the start and the end and a linear acceleration/deceleration, in between.

A pulse output pattern depends on parameters entered in registers R1 to R7 and R14 and R15. Also, if a moving amount is too small in preset mode operation, a maximum pulse rate is automatically lowered to permit smooth S-curve acceleration/deceleration. In this case, the smaller the moving amount, the shorter the linear acceleration/deceleration section and if the linear section is zero, the S-curve section is made shorter. The FH rate correction function can be turned off as required.

Pulse Output Pattern with S-curve Acccceleration/Deceleration



FH Rate Correction Function



Automatic Adjustment of Maxium Pulse Rate
Based on Moving Amount (Number of Output Pulses)

5.1.1 Multiplication Parameter [16-bit R7 Register]

Write the multiplication parameter to the R7 register in a range of 2 to 65,536 ($FFFF_{HEX}$). The parameter will determine the factor to multiply the pulse rates entered in registers R1, R2 and R3. The higher the multiplication factor, the coarser the selectable pulse rate steps. Usually therefore, a smaller multiplication factor is used. Relations between the R7 value and a multiplication factor are expressed with the following equation:

$$\text{R7 value} = \frac{\text{Reference clock (Hz)}}{\text{(Multiplication factor) x 8192}}$$

Examples with a reference clock of 4.9152MHz

R7 Value	Multiplication Factor	Output Pulse Rate (pps)
60000 ($0EA60_{HEX}$)	0.01	0.01 to 81.91
30000 (7530_{HEX})	0.02	0.02 to 163.82
12000 ($2EE0_{HEX}$)	0.05	0.05 to 409.55
6000 (1770_{HEX})	0.1	0.1 to 819.1
3000 ($0BBB_{HEX}$)	0.2	0.2 to 1638.2
1200 ($4B0_{HEX}$)	0.5	0.5 to 4095.5
600 (258_{HEX})	1	1 to 8191
300 ($12C_{HEX}$)	2	2 to 16382
120 (78_{HEX})	5	5 to 40955
60 ($3C_{HEX}$)	10	10 to 81910
30 ($1E_{HEX}$)	20	20 to 163820
12 ($0C_{HEX}$)	50	50 to 409550
6 (6_{HEX})	100	100 to 819100
2 (2_{HEX})	300	300 to 2457300

To obtain a maximum output pulse rate of 50 kpps with 5,000 entered in the R1, R2 or R3 register, for example, enter 60 in the R7 register to multiply the pulse rate by 10 times.

5.1.2 FL Pulse Rate [13-bit R1 Register]

Write the FL pulse rate to the R1 register in a range of 1 to 8,191 ($1FFF_{HEX}$). The rate will be multiplied by the multiplication factor determined by the R7 value to be used for constant-speed operation or at the start and end of varied-speed operation.

$$\text{R1 value} = \frac{\text{Output pulse rate (pps)}}{\text{Mutiplication factor}}$$

e.g. To obtain an output pulse rate of 100 pps through 10 times multiplication, write 10 to the R1 register.

5.1.3 FH1 Pulse Rate [13-bit R2 Register]

Write the FH1 pulse rate to the R2 register in a range of 1 to 8,191 ($1FFF_{HEX}$). The rate will be multiplied by the multiplication factor determined by the R7 register to be used for constant-speed or varied-speed operation. For varied-speed operation, the FH1 pulse rate should be higher than the FL pulse rate.

$$\text{R2 value} = \frac{\text{Output pulse rate (pps)}}{\text{Mutiplication factor}}$$

e.g. To obtain an output pulse rate of 50 kpps through 10 times multiplication, write 5000 to the R2 register.

5.1.4 FH2 Pulse Rate [13-bit R3 Register]

Write the FH2 pulse rate to the R3 register in a range of 1 to 8,191 ($1FFF_{HEX}$). The rate will be multiplied by the multiplication factor determined by the R7 register to be used for constant-speed or varied-speed operation. For varied-speed operation, the FH2 pulse rate should be higher than the FL pulse rate. You may freely use either FH1 or FH2 pulse rate.

$$\text{R3 value} = \frac{\text{Output pulse rate (pps)}}{\text{Mutiplication factor}}$$

e.g. To obtain an output pulse rate of 40 kpps through 10 times multiplication, write 4000 to the R3 register.

5.1.5 Maximum Acceleration Parameter [16-bit R4 Register]

Write a maximum acceleration parameter to the R4 register in a range of 1 to 65,535 ($FFFF_{HEX}$). If the automatic ramping-down point setting function is made valid, the parameter entered here is also used for deeceleration. Relations between the R4 value and a maximum acceleration rate A_{SU} (pps/sec) are expressed with the following equation:

$$\text{R4 value} = \frac{\text{(Multiplication factor) x (Reference clock, Hz) x 2}}{\text{Maximum acceleration rate } A_{SU}}$$

e.g. To obtain a maximum acceleration rate of 100 kpps/sec through 10 times multiplication, write 983 to the R4 register.

$(10 \times 4915200 \times 2) \div 100000 = 983.$

5.1.6 Maximum Deceleration Parameter [16-bit R5 Register]

Write a maximum deceleration parameter to the R5 register in a range of 1 to 65,535 ($FFFF_{HEX}$). If the automatic ramping-down point setting function is made valid, the parameter entered here has no function and that entered in the R4 register is used for deceleration. Relations between the R5 value and a maximum deceleration rate A_{SD} (pps/sec) are expressed with the following equation, where A_{SD} is an absolute value of practical deceleration (negative).

$$\text{R5 value} = \frac{\text{(Multiplication factor) x (Reference clock, Hz) x 2}}{\text{Maximum deceleration rate } A_{SD}}$$

e.g. To obtain a maximum deceleration rate of 80 kpps/sec through 10 times multiplication, write 1229 to the R5 register.
(10 x 4915200 x 2) ÷ 80000 = 1229

5.1.7 S-curve Acceleration Section [16-bit R14 Register]

Write the S-curve acceleration section to the R14 register in a range of 1 to 4,095 (FFF_{HEX}). An S-curve acceleration will be made from the starting pulse rate (R1 value x multiplication factor) to the point [starting pulse rate + (R14 value x multiplication factor)] and from the point [target operating pulse rate − (R14 value x multiplication factor)] to the target operating pulse rate [(R2 or R3) x multiplication factor]. And a linear acceleration will be made in between.
If the R14 register is set at 0 (default), S-curve acceleration will be made based on [(operating pulse rate − starting pulse rate) ÷ 2] and no linear acceleration will be made. To put an intermediate linear acceleration, set the R14 register in a range of 1 to a value lower than [(operating pulse rate − starting pulse rate) ÷ 2]. Relations between the R14 value and an S-curve acceleration section S (pps) are expressed with the following equation:

$$\text{R14 value} = \frac{\text{S-curve acceleration section S (pps)}}{\text{(Multiplication factor)}}$$

e.g. Write 1000 to the R14 register with multiplication factor = 10, starting pulse rate = 100 pps (R1 = 10) and operating pulse rate = 50,000 pps (R2 = 5000). S will be 10,000 and an S-curve acceleration will be made in a section of 100 to 10,100 pps and in a seection of 40,000 to 50,000 pps.

5.1.8 S-curve Deceleration Section [12-bit R15 Register]

Write the S-curve deceleration section to the R15 register in a range of 1 to 4,095 (FFF_{HEX}). An S-curve deceleration will be made from the operating pulse rate to the point [operating pulse rate − (R15 value x multiplication factor)] and from the point (R15 value x multiplication factor) to the starting pulse rate. And a linear deceleration will be made in the intermediate section.
If the R15 register is set at 0 (default), S-curve deceleration will be made based on [(operating pulse rate − starting pulse rate) ÷ 2]. No linear deceleration will be made. To put an intermediate linear deceleration, set the R15 register in a range of 1 to a value lower than [(operating pulse rate − starting pulse rate) ÷ 2]. Relations between the R15 value and an S-curve deceleration section S (pps) are expressed with the following equation:

$$\text{R15 value} = \frac{\text{S-curve deceleration section S (pps)}}{\text{(Multiplication factor)}}$$

e.g. Write 1000 to the R15 register with multiplication factor = 20, starting pulse rate = 500 pps (R1 = 25) and operating pulse rate = 100,000 pps (R2 = 5000). S will be 20,000 and an S-curve deceleration will be made in a section of 100,000 to 80,000 pps and in a seection of 20,500 to 500 pps.

5.1.9 Acceleration/Deceleration Time

You can obtain the acceleration/deceleration time based on values entered in registers R1 to R5 and R14 and R15. The equation differs depending on the acceleration/deceleration mode as follows:

(1) S-curve Acceleration/Deceleration with No Intermediate Linear Section

$$\text{Acceleration time } T_{SU}\text{ (s)} = \frac{(R2 - R1) \times R4}{\text{Reference clock (Hz)}}$$

$$\text{Deceleration time } T_{SD}\text{ (s)} = \frac{(R2 - R1) \times R5}{\text{Reference clock (Hz)}}$$

(2) S-curve Acceleration/Deceleration with Intermediate Linear Section

$$\text{Acceleration time } T_{SU}\text{ (s)} = \frac{(R2 - R1 + R14 \times 2) \times R4}{\text{Reference clock (Hz)} \times 2}$$

$$\text{Deceleration time } T_{SD}\text{ (s)} = \frac{(R2 - R1 + R15 \times 2) \times R5}{\text{Reference clock (Hz)} \times 2}$$

Substitute R3 for R2 if you use the R3 register for the operating pulse rate. Also, if the automatic ramping-down point setting function is made valid, substitute R4 for R5, since the R4 value is used in place of the R5 value for deceleration.

5.1.10 Ramping-down Point [24-bit R6 Register]

For varied-speed operation in the preset mode, write the ramping-down starting point (number of total pulses output before stop) to the R6 register in a range of 0 to 16,777,215 ($FFFFF_{HEX}$).

The LSI provides the automatic ramping-down point setting function which can be made valid or invalid by the control mode command bit 4. If the function is made valid, the R6 value is offset from the automatic setting value. A resultant positive value starts ramping-down earlier and a negative value delays ramping-down. In the case of automatic setting, reset the R6 register once with the clear command, and then write the ramping-down point to the R6 register in a range of −8,388,608 (800000_{HEX}) to +8,388,607 ($8FFFFF_{HEX}$).

If the automatic setting function is made invalid, the ramping-down point entered in the R6 register is used as it is.

- For normal operation of the automatic ramping-down point setting function, the time T_{SDB} from the start of acceleration to the start of deceleration should be equal to or longer than the deceleration time T_{SD}. Generally, the R14 value should be equal to or longer than the R15 value. (See the pulse output pattern with S-curve acceleration/deceleration on page 19.
- For the manual setting of ramping-down point, use the following procedure to obtain the value to be entered in the R6 register. If you use the FH2 pulse rate, substitue R3 for R2 in the equations below.

5.1.10.1 S-curve Acceleration/Deceleration with No Linear Section

(1) Make sure of the trapezoidal motion profile pulse output pattern.
If the moving amount is too small, acceleration is not available to the FH pulse rate, thereby resulting in a triangular motion profile pattern.

Minimum number of output pulses required for trapezoidal profile

$$= \frac{(R2^2 - R1^2) \times (R4 + R5)}{R7 \times 16384}$$

(2) Revise FH pulse rate.
If a preset number of output pulses (R0) is equal to or lower than a minimum number of output pulses, a triangular pattern results. Therefore, revise the FH pulse rate required for the trapezoidal profile.

$$\text{Revised FH pulse rate (R2)} = \sqrt{\frac{R0 \times R7 \times 16384}{R4 + R5} + R1^2}$$

(3) Write the ramping-down point to the R6 register.

$$\text{Ramping-down point (R6)} = \frac{(R2^2 - R1^2) \times R5}{R7 \times 16384}$$

5.1.10.2 S-curve Acceleration/Deceleration with Linear Section

(1) Make sure of the trapezoidal motion profile pulse output pattern.
If the moving amount is too small, acceleration is not available to the FH pulse rate, thereby resulting in a triangular pattern.

Minimum number of output pulses required for trapezoidal pattern

$$= \frac{(R1 + R2) \times [(R2 - R1) \times (R4 + R5) + 2 \times (R4 \times R14 + R5 \times R15)]}{R7 \times 32768}$$

(2) Make sure of the linear acceleration/decleration section.
If a preset number of output pulses (R0) is equal to or lower than a minimum number of output pulses required for the trapezoidal pattern, make sure that a linear acceleration/deceleration section is available.

[In the case of R14 = R15]

Minimum number of output pulses required
to put an intermediate linear acceleration/deceleration section

$$= \frac{(R1 + R14) \times R14 \times (R4 + R5)}{R7 \times 4096}$$

[In the case of R14 > R15]

Minimum number of output pulses required
to put an intermediate linear acceleration/deceleration section

$$= \frac{(R1 + R14) \times [R5 \times (R14 + R15) + 2 \times R4 \times R15]}{R7 \times 8192}$$

In the case of R14 < R15:

Minimum number of output pulses required to put an intermediate linear acceleration/deceleration section

$$= \frac{(R1 + R15) \times [R4 \times (R14 + R15) + 2 \times R5 \times R15]}{R7 \times 8192}$$

(3) Revise the FH pulse rate.

If a minimum number of output pulses required to put an intermediate acceleration/deceleration section is lower than the preset number of output pulses (R0), and the R0 value is equal to or lower than a minimum number of output pulses required for a trapezoidal pattern, revise the FH pulse rate to avoid a triangular pattern.

In the case of R14 = R15:

Revised FH pulse rate (R2) =

$$R14 + \sqrt{(R14 - R1)^2 - \frac{R0 \times R7 \times 32768}{R4 + R5}}$$

In the case of R14 o R15:

Revised FH pulse rate (R2) =

$$\frac{-A + \sqrt{(A - B \times R1)^2 + (B \times R0 \times R7 \times 32768)}}{B}$$

Where, A = R4 x R14 + R5 x R15

B = R4 + R5

If the preset number of output pulses (R0) is equal to or lower than a minimum number of output pulses required to put an intermediate linear acceleration/deceleration section, enter 0 in R14 and R15 registers to effect the S-curve acceleration/deceleration mode with no intermediate linear section, and follow instructions of 5.1.10.1.

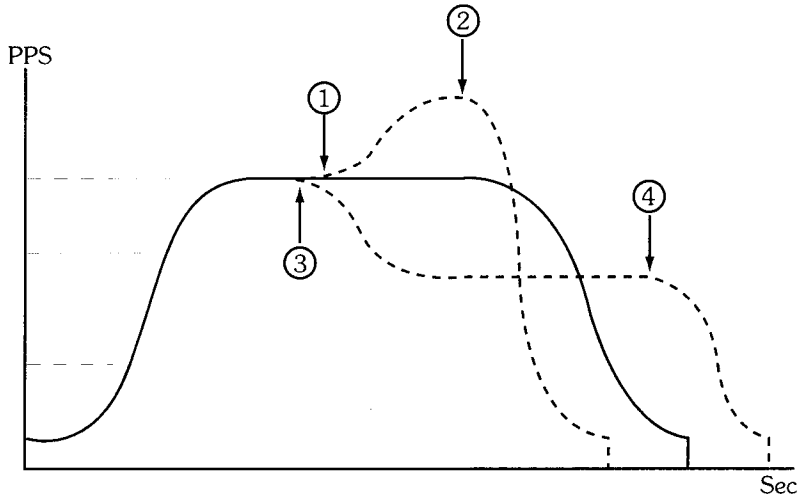
(4) Write the ramping-down point to the R6 register.

$$\text{Ramping-down point (R6)} = \frac{(R1 + R2) \times (R2 - R1 + R15 \times 2) \times R5}{R7 \times 32768}$$

5.1.11 Changing Pulse Output Pattern in Motion

You can change the pulse output speed during pulse output in progress by revising the FH pulse rate. However, if the automatic ramping-down point setting function is made valid, do not revise parameters entered in R1, R4, R5, R14 and R15 registers during operation. The automatic ramping-down point setting function cannot follow the revision.

Examples of Changing Pulse Output Pattern in Motion in Preset Mode



1) ① The operation speed is increased due to revision of the R2 or R3 value to a higher pulse rate.
(FH1 or FH2 varied-speed start command)
② Ramping-down starts automatically at the ramping-down point.
2) ③ The operation speed is decreased due to revision of the R2 or R3 value to a lower pulse rate.
(FH1 or FH2 varied-speed start command)
④ Ramping-down starts automatically at the ramping-down point.

5.2 Bits of Command Buffer

To operate the LSI, you need to write data to the command buffer and registers through the 8-bit data bus. Commands are classified into four types by high-place two bits as in the chart below. The LSI provides the command buffer to hold the content of each type of command and to retain the content until the next command of same type is written.

Each command is not a code but provides functions by bits. Therefore, you can set a command other than exampled in this manual.

Writing the start mode command starts the LSI generating pulses. Therefore, write this command at the end.

Besides the command buffer, the LSI provides extension mode registers R12 and R13. Note, however, that the extension mode registers cannot be used if the LSI is placed in the interchangeable mode with the 240K.

D7	D6	D5	D4	D3	D2	D1	D0
C1	C0						

C1	C0	Type of Command
0	0	Stard mode
0	1	Control mode
1	0	Register select
1	1	Output mode

5.2.1 Start Mode Command

D7	D6	D5	D4	D3	D2	D1	D0
0	0						

Pulse Rate (Speed) Selection
D1 D0
0 0 : FL pulse rate
0 1 : FH1 pulse rate
1 0 : FL pulse rate
1 1 : FH2 pulse rate

Pulse Output Mode
0: Constant speed 1: Varied speed

Stop Control
0: OFF 1: ON

Start Control
0: OFF 1: ON

$\overline{\text{INT}}$ Output at the Stop
0: No ($\overline{\text{INT}}$ reset) 1: Yes

Pulse Rate Selection (Bits 1 and 0)

Select the R1, R2 or R3 register, the pulse rate of which you want to use, by entering 00, 01 or 11 in these bits. The output pulse rate is a product of the parameter written in the register and the multiplication factor determined by the R7 register.

Pulse Output Mode (Bit 2)

Enter 0 in bit 2. The LSI will output pulses at a fixed rate selected by bits 1 and 0. In constant-speed operation, $\overline{SD\pm}$ signals and ramping-down point setting in the R6 register have no function.

Enter 1 in bit 2. The LSI will output pulses while accelerating the rate from the FL to FH rate at the start and decelerating it from the FH to FL rate before stop. In varied-speed operation $\overline{SD\pm}$ signals and the ramping-down point setting for the preset mode have respective functions.

Start/Stop Control (Bit 4 or 3)

Enter 1 in bit 4 to start the LSI generating pulses and enter 1 in bit 3 to stop it. By using bits 4 and 3 in combination, you can perform deceleration-stop.

$\overline{INT}$ Output at the Stop (Bit 5)

Enter 1 in bit 5. The $\overline{INT}$ signal will be output when the LSI will stop generating pulses due to completion of the preset mode operation, the $\overline{EL\pm}$, $\overline{ORG}$ $\overline{or\ ALM}$ signal or the stop command.

To reset the $\overline{INT}$ signal, set bit 5 at 0. Also, if you want to mask the $\overline{INT}$ signal at the time of stop, set bit 5 at 0.

In the standard mode the LSI can output the $\overline{INT}$ signal at the ramping-down point with bit 13 of R12 register set at 1.

The $\overline{INT}$ pin outputs a logical sum—the interrupt signal due to stop or ramping-down point. To find which factor causes the $\overline{INT}$ signal, check the extension status register.

Clear Command

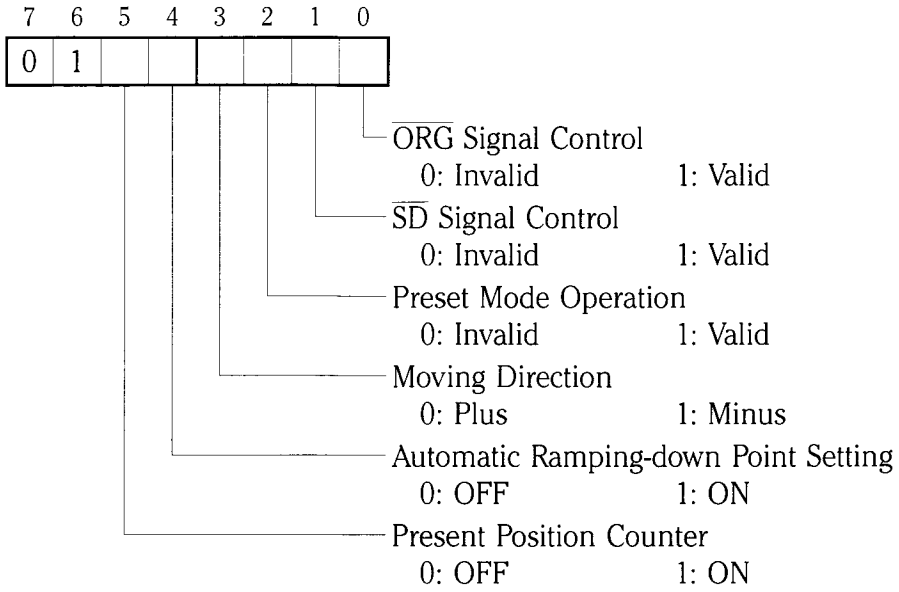
The LSI provides a latch to hold the stop condition. Therefore, to start the LSI generating pulses anew, you need to reset the latch. Enter 0 in bit 4 of the start mode command. The latch will be reset. Before starting, write the clear command (typically, 08_{HEX} for immediate stop). The clear command will also be used to reset the ramping-down point counter if the automatic ramping-down point setting function is made valid.

Typical Settings of Start Mode Command

D7	D6	D5	D4	D3	D2	D1	D0	HEX	Description
0	0	0	1	0	0	0	0	10	Constant-speed operation at FL rate with no $\overline{INT}$ signal at the stop
0	0	1	1	0	0	0	0	30	Constant-speed operation at FL rate with the $\overline{INT}$ signal at the stop
0	0	0	1	0	0	0	1	11	Constant-speed operation at FH1 rate with no $\overline{INT}$ signal at the stop
0	0	0	1	0	1	0	1	15	Constant-speed operation at FH2 rate with no $\overline{INT}$ signal at the stop
0	0	0	1	0	1	1	1	15	Varied-speed operation with no $\overline{INT}$ signal at the stop; acceleration from FL to FH1 rate
0	0	0	1	0	1	1	1	17	Varied-speed operation with no $\overline{INT}$ signal at the stop; acceleration from FL to FH2 rate
0	0	0	1	0	1	0	0	14	Deceleration on the way with no $\overline{INT}$ signal at the stop: deceleration from FH1 or FH2 to FL rate
0	0	0	1	1	1	1	1	1F	Deceleration-stop with no $\overline{INT}$ signal at the stop; Stop when the FL rate is reached through deceleration from the FH rate (clear command required after stop)
0	0	1	1	1	1	1	1	3F	Deceleration-stop with the $\overline{INST}$ signal at the stop
0	0	0	0	1	0	0	0	08	Immediate stop (= clear command) with no $\overline{INT}$ signal at the stop
0	0	1	0	1	0	0	0	28	Immediate stop with the $\overline{INT}$ signal at the stop

Note: FL, FH1 and FH2 rates here are output pulse rates (pulse rates written to R1, R2 and R3 registers x the multiplication factor determined by the R7 value).

5.2.2 Control Mode Command



ORG Signal Control (Bit 0)

You can select whether the ORG signal stops the LSI from generating pulses or not.

Enter 1 in bit 0. Putting the ORG pin at low level will immediately stop the LSI from generating pulses. This function is useful for origin return. Origin return is also available with a combination of the ORG signal and Z-phase signal.

Enter 0 in bit 0. The ORG pin will have no function. However, you can monitor the ORG signal using the status buffer.

SD Signal Control (Bit 1)

You can select whether SD ± signal decelerates the output pulse rate or not.

Enter 1 in bit 1. Putting the SD pin in the moving direction at low level will decelerate the output pulse rate from FH to FL, and the LSI will keep generating pulses at the FL rate until the SD signal will recover high level.

Enter 0 in bit D1. SD ± pins will have no function. However, you can check the SD signal ON/OFF status with the extension status register.

Preset Mode Operation (Bit 2)

Enter 1 in bit 2 with a desired number of pulses written to the preset counter (R0 register). The start mode command will start the LSI generating pulses while letting the preset counter count down by every pulse output. When the counter value becomes equal to or higher than the ramping-down point value set in the R6 register, the LSI will decelerate the output pulse rate and stop generating pulses when the counter counts down to 0.

If you enter 0 in bit 2, the preset counter counts down but the LSI does not stop generating pulses when the counter counts down to 0.

Moving Direction (Bit 3)

You can select the direction of output pulses. Enter 0 in bit 3 to select plus direction pulses and enter 1 to select minus direction pulses. For relations between the direction signal pin and the pulse output pin, refer to "5.4.2 Pulse Output Mode."

Setting of this bit is related with the direction of $\overline{EL\pm}$ and $\overline{SD\pm}$ signals.

Automatic Ramping-down Point Setting (Bit 4)

Enter 0 in bit 4. The ramping-down point will be as written to the R6 register.

Enter 1 in bit 4. The ramping-down point will be automatically calculated during acceleration and pulse output at the FH rate. If a parameter is written to the R6 register, the value is added to the automatically calculated value to make a ramping-down point.

Present Position Counter (Bit 5)

You can turn the present position counter on or off.

Enter 1 in bit 5. The present position counter will count up by every output of plus direction pulse or will count down by every output of minus direction pulse.

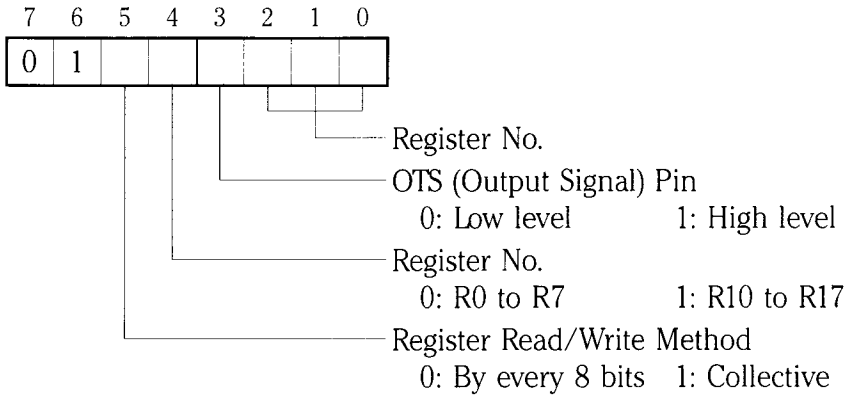
Enter 0 in bit 5. The present position counter will not operate.

For the continuous mode, preset mode and origin return, refer to "5.3 Operation Modes."

Typical Settings of Start Mode Command (Mark "—" in the table may be 0 or 1.)

D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	—	—	—	—	0	Makes $\overline{\text{ORG}}$ signal control invalid.
0	1	0	—	—	—	—	1	Makes $\overline{\text{ORG}}$ signal control valid.
0	1	0	—	—	—	0	—	Makes $\overline{\text{SD}}$ signal control invalid.
0	1	0	—	—	—	1	—	Makes $\overline{\text{SD}}$ signal control valid (in varied-speed operation).
0	1	0	—	—	0	—	—	Makes preset counter control invalid.
0	1	0	—	—	1	—	—	Makes preset counter control valid.
0	1	0	—	0	—	—	—	Selects plus direction pulses.
0	1	0	—	1	—	—	—	Selects minus direction pulses.
0	1	0	0	—	—	—	—	Ramping-down point = R6 value
0	1	0	1	—	—	—	—	Automatically sets the ramping-down point.
0	1	0	—	—	—	—	—	Turns present position counter OFF.
0	1	1	—	—	—	—	—	Turns present position counter ON.
0	1	0	—	—	0	0	0	Selects continuous mode with $\overline{\text{SD}}$ signal control invalid.
0	1	0	—	—	0	1	0	Selects continuous mode with $\overline{\text{SD}}$ signal control valid.
0	1	0	—	—	0	0	1	Selects origin return mode with $\overline{\text{SD}}$ signal control invalid.
0	1	0	—	—	0	1	1	Selects origin return mode with $\overline{\text{SD}}$ signal control valid.
0	1	0	—	—	1	0	0	Selects preset mode with $\overline{\text{ORG}}$ and SD signal control invalid.
0	1	0	—	—	1	1	0	Selects preset mode with $\overline{\text{SD}}$ signal control invalid.
0	1	0	—	—	1	1	1	Selects preset mode with $\overline{\text{ORG}}$ and SD signal control valid.

5.2.3 Register Select Command



Register No. (Bits 4, 2, 1 and 0)

Using these bits, you need to select the register before reading or writing data from/to it. For types of registers and selection parameters, refer to the tables on the next page. If you place the LSI in the interchangeable mode with the 240K, you cannot select any of registers R10 to R17.

OTS (Output Signal; Bit 3)

You can control the general-purpose OTS pin.

Enter 1 in bit 2. The OTS pin will be put at low level. Enter 0 in bit 2. The OTS pin will be put at high level.

Register Read/Write Method (Bit 5)

You can read or write data from/to a register by every 8 bits or by all 24 bits in a lump. Refer to page 14.

Enter 1 in bit 3. The register data in its full bit length will be read or written at the same timing through the 24-bit latch buffer.

When reading, the register data are once copied to the reading buffer at the time of writing the register select command and then transferred from the buffer to the CPU.

When writing, high- and middle-place data from the CPU are once latched in the writing buffer and are transferred from the buffer to the register at the time the low-place 8-bit data are written. Therefore, write data to high-, middle- and low-place bits in that order.

Note that during status reading, the status data are latched.

Enter 0 in bit 3. You can access every 8 bits individually. It is recommended not to read or write data by every 8 bits during pulse output in progress. If you do so, internal timing shifts adversely.

List of Registers

D4	D2	D1	D0	R No.	Content	Setting Range	Bit Length	R/W
0	0	0	0	R0	Preset amount	1 to 16,777,215 (FFFFFF)	24	R/W
0	0	0	1	R1	FL pulse rate	1 to 8,191 (1FFF)	13	R/W*
0	0	1	0	R2	FH1 pulse rate	1 to 8,191 (1FFF)	13	R/W*
0	0	1	1	R3	FH2 pulse rate	1 to 8,191 (1FFF)	13	R/W*
0	1	0	0	R4	Accleration rate	2 to 65,535 (FFFF)	16	R/W*
0	1	0	1	R5	Deceleration rate	2 to 65,535 (FFFF)	16	R/W*
0	1	1	0	R6	Ramping-down point	0 to 16,777,215 (FFFFFF)	24	R/W*
0	1	1	1	R7	Magnification factor	2 to 65,535 (FFFF)	16	R/W*
1	0	0	0	R10	Present position Counter	0 to 16,777,215 (FFFFFF)	24	R/W
1	0	0	1	R11	Present rate monitor	1 to 8,191 (1FFF)	13	R
1	0	1	0	R12	Extension mode 1		24	R/W
1	0	1	1	R13	Extension mode 2		24	R/W
1	1	0	0	R14	S-curve accel section	0 to 4,095 & control bit 1	16	R/W
1	1	0	1	R15	S-cruve decel section	0 to 4,095 (FFF)	12	R/W
1	1	1	0	R16	Command buffer monitor		24	R
1	1	1	1	R17	Extension status		21	R

*Write only in the interchangeable mode with the 240K.

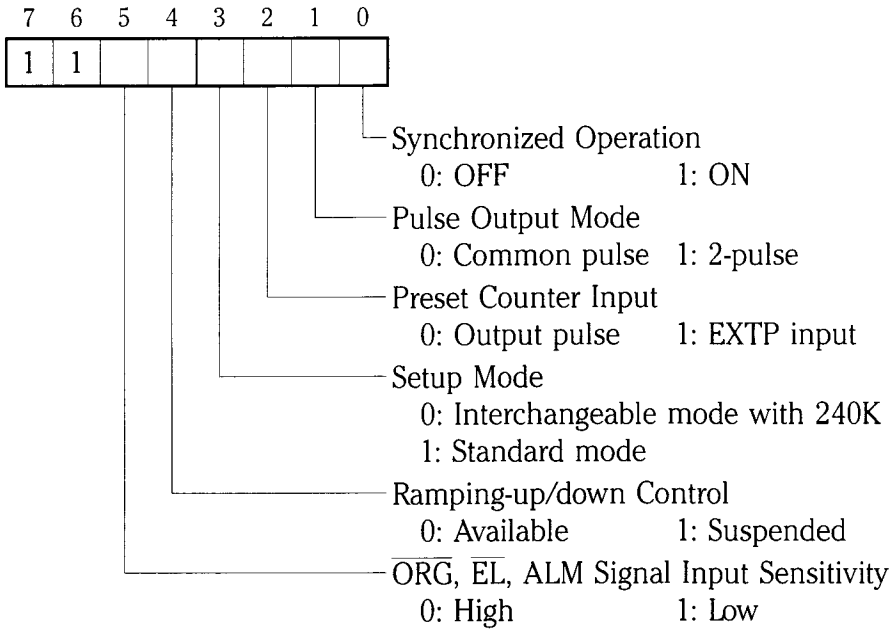
Note: Read/write from/to Registers R10 to R17 are not availalble in the interchangeable mode with the 240K.

Typical Settings of Register Select Command

(Mark "—" may be 0 or 1.)

D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	—	0	—	0	0	0	Selects R0 register.
1	0	—	0	—	0	0	1	Selects R1 register.
1	0	—	0	—	0	1	0	Selects R2 register.
1	0	—	0	—	0	1	1	Selects R3 register.
1	0	—	0	—	1	0	0	Selects R4 register.
1	0	—	0	—	1	0	1	Selects R5 register.
1	0	—	0	—	1	1	0	Selects R6 register.
1	0	—	0	—	1	1	1	Selects R7 register.
1	0	—	1	—	0	0	0	Selects R10 register.
1	0	—	1	—	0	0	1	Selects R11 register.
1	0	—	1	—	0	1	0	Selects R12 register.
1	0	—	1	—	0	1	1	Selects R13 register.
1	0	—	1	—	1	0	0	Selects R14 register.
1	0	—	1	—	1	0	1	Selects R15 register.
1	0	—	1	—	1	1	0	Selects R16 register.
1	0	—	1	—	1	1	1	Selects R17 register.
1	0	—	—	0	—	—	—	Puts OTS pin at low level.
1	0	—	—	1	—	—	—	Puts OTS pin at high level.
1	0	0	—	—	—	—	—	Read/write by every 8 bits.
1	0	1	—	—	—	—	—	Read/write by all 24 bits in a lump.

5.2.4 Output Mode Command



Synchronized Operation (Bit 0)

Synchronized operation here means that two or more LSIs are operated in synchronization for simultaneous start/stop, etc.

Enter 1 in bit 0. The SYN1 pin for synchronization signal input will be valid.

Pulse Output Mode (Bit 1)

You can select either the common pulse mode or the 2-pulse mode.

Enter 0 in bit 1 to select the common pulse mode. The $\overline{\text{POUT}}$ will output command pulses while the PDIR pin will output the direction signal. The direction signal at high level indicates plus direction and the direction signal at low level indicates minus direction.

Enter 1 in bit 1 to select the 2-pulse mode. The $\overline{\text{POUT}}$ pin will output command pulses in plus direction and the PDIR pin will output command pulses in minus direction.

Using the extension mode register 1, you can change the output logic of $\overline{\text{POUT}}$ and PDIR pins.

Preset Counter Input (Bit 2)

You can select the type of pulses to be counted by the preset counter R0.

Enter 0 in bit 2. The preset counter will count pulses output from the $\overline{\text{POUT}}$/PDIR pin.

Enter 1 in bit 2. The preset counter will count pulses input from the EXTP pin. You can stop it from counting by fixing the $\overline{\text{EXTP}}$ to high level.

Setup Mode (Bit 3)

You can place the LSI in either interchangeable mode with the 240K or the standard mode which makes registers R10 to R17 usable.

Enter 1 in bit 3. The LSI will be placed in the standard mode. In the standard mode you can use the enhanced functions such as the present position counter, servo control signals $\overline{INP}$, $\overline{CLR}$ and ALM, Z-phase signal based origin return, S-curve acceleration/deceleration with an intermediate linear section, monitoring command/extension status and read/write of register data by all 24 bits in a lump.

Enter 0 in bit 3. The LSI will be placed in the interchangeable mode with the 240K. In the interchangeable mode with the 240K, you cannot write data to registers R10 to R17 and can read data only from the status buffer and the R0 register.

With any mode selected, acceleration/deceleration in varied-speed operation will be made in an S curve.

Ramping-up/down Control (Bit 4)

Enter 1 in bit 4 during acceleration/deceleration in progess. The LSI will stop acceleration/deceleration and will output pulses at the rate used on the way of acceleration/deceleration. You can check the rate by reading the R11 register (present pulse rate monitor).

Enter 0 in bit 4 thereafter. The LSI will restart acceleration/deceleration.

For usual operation, set the bit at 0.

$\overline{ORG}$, $\overline{EL}$ and ALM Signal Input Sensitivity (Bit 5)

You can select the input sensitivity of $\overline{ORG}$, $\overline{EL}$ and ALM signals.

Enter 1 in bit 5. The input sensitivity of these signals will be low and signals with a pulsewidth shorter than four cycles of the reference clock (approximately 800ns with a reference clock of 4.9152MHz) will not be accepted.

Enter 0 in bit 5. The input sensitivity of these signals will be high and a signal with a pulsewidth of 50ns or so will be accepted.

Select the high sensitivity if you use $\overline{EC\text{-}Z}$ signals for counting to complete an origin return.

Typical Settings of Output Mode Command (Mark "—" may be 0 or 1.)

D7	D6	D5	D4	D3	D2	D1	D0	Description
1	1	—	—	—	—	—	0	Makes synchronized operation unavailable.
1	1	—	—	—	—	—	1	Makes synchronized operation available.
1	1	—	—	—	—	0	—	Selects the command pulse mode.
1	1	—	—	—	—	1	—	Selects the 2-pulse mode.
1	1	—	—	—	0	—	—	Lets the preset counter count pulses output from the $\overline{\text{POUT}}$/PDIR pin.
1	1	—	—	—	1	—	—	Lets the preset counter count pulses input from the EXTP pin.
1	1	—	—	0	—	—	—	Selects the interchangeable mode with 240K.
1	1	—	—	1	—	—	—	Selects the standard mode.
1	1	—	0	—	—	—	—	Makes acceleration/deceleration available.
1	1	—	1	—	—	—	—	Suspends acceleration/deceleration.
1	1	0	—	—	—	—	—	Selects high input sensitivity for $\overline{\text{ORG}}$, $\overline{\text{EL}}$ and ALM signals.
1	1	1	—	—	—	—	—	Selects low input sensitivity for $\overline{\text{ORG}}$, $\overline{\text{EL}}$ and ALM signals.

5.3 Operation Modes

Set the operation mode using the control mode command and extension mode registers. In varied-speed operation, the $\overline{SD}$ signal in the moving direction starts the LSI decelerating the pulse output and in any mode other than timer mode, the $\overline{EL}$ signal in the moving direction and ALM signal stop the LSI from generating pulses.

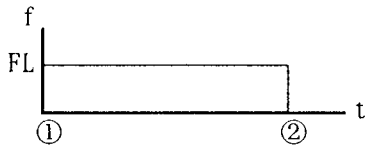
5.3.1 Continuous Mode

Writing the start mode command starts the LSI generating pulses in the direction designated by bit 3 of the control mode command and lets it continue generating pulses until receiving the stop command. The preset counter counts down even in continuous mode operation.

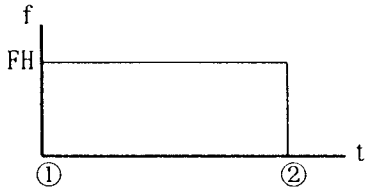
Place the LSI in the continuous mode by making the $\overline{ORG}$ signal control and the preset mode operation control invalid with the control mode command.

Setting—

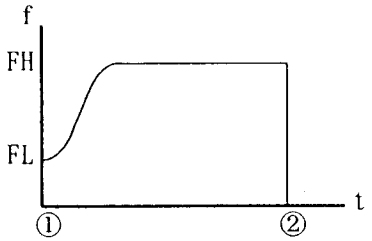
Control mode command: Bit 2 = 0 (preset mode operation invalid)
Bit 0 = 0 ($\overline{ORG}$ signal control invalid)



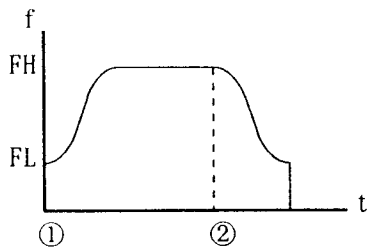
① Start mode command (10HEX) written for constant speed operation at FL rate
② Immediate stop command (08HEX) written



① Start mode command (11HEX) written for constant speed operation at FH1 rate
② Immediate stop command (08HEX) written



① Start mode command (15HEX) written for varied-speed operation at FH1 rate
② Immediate stop command (08HEX) written



① Start mode command (17HEX) written for varied-speed operation at FH2 rate
② Deceleration-stop command (1FHEX) written

5.3.2 Preset Mode

Enter the number of output pulses in the R0 register (preset counter) and designate the moving direction by setting bit 3 of the control mode command. The R0 register will count down from the preset number and the LSI will stop generating pulses when the R0 register will count down to 0. The R0 register can be set in a range of 1 to 16,777,215.

To place the LSI in the preset mode, make the preset mode operation control valid and lets the preset counter count pulses output from the $\overline{\text{POUT}}$/PDIR pin.

Settings—

Control mode command: Bit 2 = 1 (preset mode)
Output mode command: Bit 2 = 1 (counting output pulses)

5.3.3 Origin Return Mode

There are three origin return conditions: (1) $\overline{\text{ORG}}$ signal, (2) $\overline{\text{ORG}}$ signal + Z-phase signal/s to the number selectable in a range of 1 to 16, (3) $\overline{\text{SD}}$ signal + Z-phase signal/s to the number selectable in a range of 1 to 16. The Z-phase signal is the encoder marker signal and is usually output one pulse per revolution. Using the Z-phase signal, you can increase the accuracy of origin return. The LSI inputs the Z-phase signal through the $\overline{\text{EC-Z}}$ pin.

The $\overline{\text{ORG}}$ signal with a pulsewidth of 50nS or so can stop the LSI from generating pulses. But you can cancel $\overline{\text{ORG}}$ signals with a pulsewidth of shorter than four cycles of the reference clock (800nS with a reference clock of 4.9152MHz) by turning the input filter on with the output mode command. If you use the Z-phase signal in combination, do not turn the input filter on.

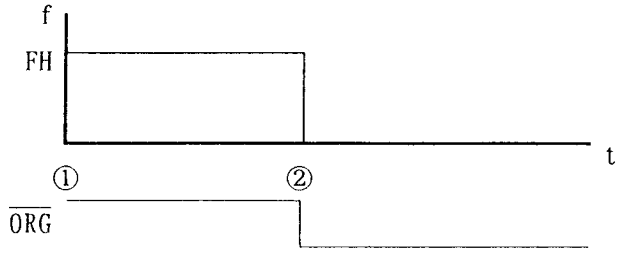
5.3.3.1 To Stop with $\overline{\text{ORG}}$ Signal Only

"$\overline{\text{ORG}}$ signal ON" stops the LSI from generating pulses. Then. bit 10 of the extension status register R17 becomes 1 to indicate that the factor that stopped the LSI from generating pulses is "$\overline{\text{ORG}}$ signal ON." The LSI keeps stopping, though the signal is turned off.

If the start mode command is written with the $\overline{\text{ORG}}$ signal turned on, the LSI does not generate any pulse, keeping the suspended condition. But bit 10 of the extension status register does not become 1 and no $\overline{\text{INT}}$ signal is generated. If the $\overline{\text{ORG}}$ signal is turned off, the LSI starts generating pulses.

Settings—

Control mode command: Bit 0 = 1 ($\overline{\text{ORG}}$ signal control valid)
Output mode command: No restriction
Extension mode register 2: Bit 21 = 0 ($\overline{\text{ORG}}$ signal only)



① Start mode command (11HEX) written for constant-speed operation at FH1 rate
② $\overline{ORG}$ signal turned ON

5.3.3.2 To Stop with $\overline{ORG}$ Signal + Z-phase Signals

The LSI stops generating pulses when inputting the (nnnn + 1)th $\overline{EC\text{-}Z}$ signal after the $\overline{ORG}$ signal is turned on. During the time, the $\overline{ORG}$ signal should be kept turned on.

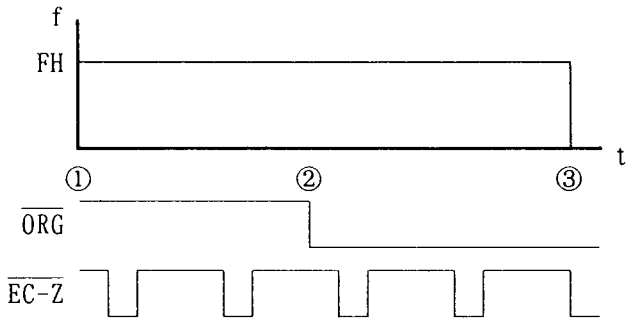
If the start mode command is written with the $\overline{ORG}$ signal turned on, the another $\overline{EC\text{-}Z}$ signal input will stop the LSI from generating pulses. Then bit 10 of the extension status register becomes 1 indicating the factor that stopped the LSI is "$\overline{ORG}$ signal turned ON."

Settings—

Control mode command: Bit 0 = 1 ($\overline{ORG}$ signal control valid)
Output mode command: Bit 5 = 0 (standard mode)
Bit 3 = 1 (high input sensitivity)

Extension mode register 2:
Bit 21 = 1 (counting Z-phase signal)
Bit 20 = 1 (timing to count Z-phase signal: $\overline{ORG}$ signal ON)
Bits D19-D16 = nnnn

If nnnn = 0010,



① Start mode command (11HEX) written for constant-speed operation at FH1 rate
② $\overline{ORG}$ signal turned ON
③ Third $\overline{EC\text{-}Z}$ signal turned ON after $\overline{ORG}$ signal

5.3.3.3 To Stop with $\overline{SD}$ Signal + Z-phase Signals

In varied-speed operation, the $\overline{SD}$ signal ON lets the LSI decelerate, and then the (nnnn + 1)th $\overline{EC\text{-}Z}$ signal input stop the LSI. The $\overline{SD}$ signal should be kept "ON" during the time.

If the start mode command is written with the $\overline{SD}$ signal turned on, another $\overline{EC\text{-}Z}$ signal input will stop the LSI from generating pulses. Then bit 10 of the extension status register becomes 1 indicating the factor that stopped the LSI "$\overline{ORG}$ signal turned ON."

If the $\overline{SD}$ signal is selected for origin return, the $\overline{ORG}$ signal has no function to stop the LSI from generating pulses.

Settings—

Control mode command: Bit 1 = 1 ($\overline{ORG}$ signal control valid)
Bit 0 = 1 ($\overline{SD}$ signal control valid)

Output mode command: Bit 5 = 0 (standard mode)
Bit 3 = 1 (high input sensitivity)

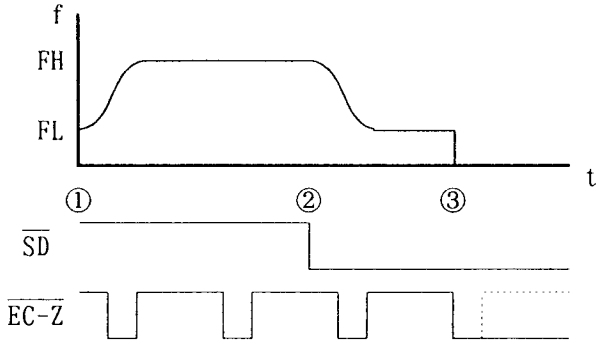
Extension mode register 2:

Bit 21 = 1 (counting Z-phase signals)

Bit 20 = 0 (timing to start counting: $\overline{SD}$ signal ON)

Bits 19-16 = nnnn (number of Z-phase signals to stop pulse generation)

If nnnn = 0001,



① Start mode command (15HEX) written for varied-speed operation at FH1 rate

② $\overline{SD}$ signal turned ON

③ Second $\overline{EC\text{-}Z}$ turned ON after $\overline{SD}$ signal

Origin return is available in either the continuous mode or the preset mode. You can change the input logic of $\overline{ORG}$ signal by setting bit 23 of the extension mode register 2 and check the ON/OFF status at bit 2 of the extension status register.

The input logic of $\overline{\text{EC-Z}}$ signal can be changed by setting bit 12 of the extension mode register 1 and its ON/OFF status can be checked at bit 20 of the extension status register. The EC-Z counter value can be checked by reading bits 16 to 19 of the extension status register.
The preset counter continues counting down even during origin return in progress.

5.3.4 Timer Mode

In the time mode you can use the LSI as a timer by letting the preset counter count down from the R0 value without outputting any pulses from the $\overline{\text{POUT}}$/PDIR pin.
For masking pulse output, make EL, ORG and ALM signal control invalid, stop the present position counter with the control mode command and place the LSI in the preset mode.
Write a desired number of pulses to the R0 register and write the start mode command for constant-speed operation. The preset counter will count down from the value entered in the R0 register. Thus, the internal operation time will be, R0 value x pulse rate. That is, if the pulse rate is 1000 pps and the number of output pulses is 120, the internal operation time is 120ms.
You can check the termination of operation through the INT signal output at the stop or by monitoring the operating status on the status register.
If the common pulse mode is selected to output the direction signal from the PDIR pin, the status of PDIR pin changes according to bit 3 of the control mode command buffer.
Also, make the INP input invalid by setting bit 1 of the extension mode register 1 at 1.

Settings—

Control mode command:	Bit 5 = 0 (present position counter invalid)
	Bit 2 = 1 (preset mode ON)
Output mode command:	Bit 3 = 1 (standard mode)
	Bit 2 = 0 (counting output pulses)
Extension mode register 1:	Bit 10 = 1 (pulse output masked)
	Bit 9 = 0 ($\overline{\text{INP}}$ signal control OFF)

5.4 Control Functions

5.4.1 Servomotor Interface

The LSI provides the following three servomotor control signals:

(1) $\overline{\text{INP}}$ Signal

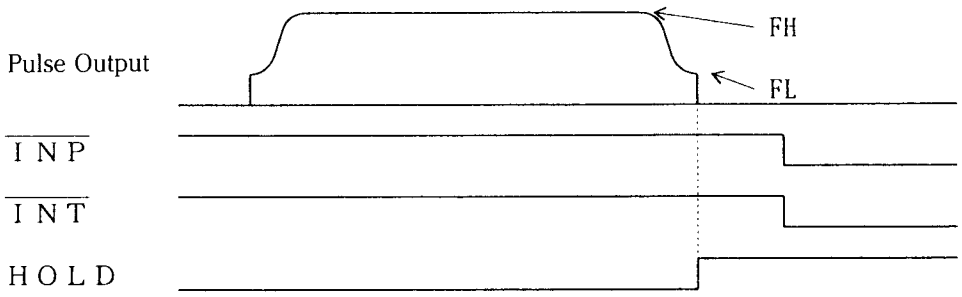
The servomotor driver outputs the in-position signal to indicate that the motor stops running. The LSI inputs this in-position signal through the $\overline{\text{INP}}$(/SYN1) pin.

Usually, the LSI stops generating pulses upon completing the total preset pulse output. But using the extension mode register 1, you can delay the output of $\overline{\text{INT}}$ signal until the $\overline{\text{INP}}$ signal is turned on. Note, however, that the output of $\overline{\text{INT}}$ signal is not delayed when the LSI stops generating pulses due to the $\overline{\text{EL}}$ or ALM signal or completion of origin return.

Though under the default condition the $\overline{\text{INP}}$ signal is negative logic, you can change it to positive logic. You can monitor the ON/OFF status.

The $\overline{\text{INP}}$ signal and the $\overline{\text{SYN1}}$ signal use the common pin.

- To use the $\overline{\text{INP}}$ signal control, set bit 9 of the extension mode register 1 at 1. $\overline{\text{INT}}$ signal output will be delayed until the $\overline{\text{INP}}$ signal will be turned on. (However, the $\overline{\text{EL}}$ or ALM signal or completion of origin return will not delay the $\overline{\text{INT}}$ signal output.)
- To change the input logic of $\overline{\text{INP}}$ signal from negative to positive, set bit 8 of the extension mode register 1 at 1.
- To select the INS pin or the $\overline{\text{INP}}$ pin for reading the status, set bit 14 of the extension mode register 2 at:
  0: INS pin
  1: $\overline{\text{INP}}$/$\overline{\text{SYN1}}$ pin
- To check the status of $\overline{\text{INP}}$/SYN1 pin, read status bit 4.
  0: $\overline{\text{INP}}$ pin = Low level
  1: $\overline{\text{INP}}$ pin = High level

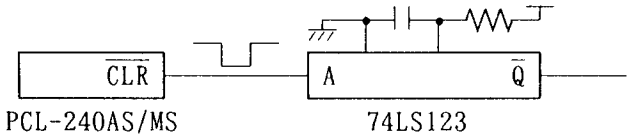


(2) $\overline{\text{CLR}}$ Signal

The $\overline{\text{CLR}}$ pin outputs a pulse signal to clear the remaining pulses in the deviation counter of servomotor driver to make the immediate stop. You can set the LSI so that it outputs the $\overline{\text{CLR}}$ signal when the $\overline{\text{EL}}$ signal is turned on or when an origin return is completed, or under manual control. For manual control, you can program the CPU to change the pulsewidth of $\overline{\text{CLR}}$ signal. But the pulsewidth is fixed to eight cycles of the reference clock (approximately 1.6μs with a reference clock of 4.9152MHz) for $\overline{\text{EL}}$signal or origin return $\overline{\text{CLR}}$.

The $\overline{\text{CLR}}$ signal and the $\overline{\text{SYN0}}$ signal use a common pin. Select the pin function as required.

According to the servomotor specification, widen the pulsewidth of $\overline{\text{CLR}}$ signal as follows:



- To select the output signal of $\overline{\text{SYN0}}$/$\overline{\text{CLR}}$ pin, set bit 4 of the extension mode register 2 at—
  - 0: $\overline{\text{SYN0}}$ signal
  - 1: $\overline{\text{CLR}}$ signal
- To make the manual $\overline{\text{CLR}}$ signal control valid or invalid, set bit 0 of the extension mode register 2 at—
  - 0: Invalid
  - 1: Valid
- To select whether the $\overline{\text{EL}}$ signal initiates the $\overline{\text{CLR}}$ signal or not, set bit 0 of the extension mode register 2 at—
  - 0: No $\overline{\text{CLR}}$ signal output when the $\overline{\text{EL}}$ signal stops the LSI from generating pulses.
  - 1: The $\overline{\text{CLR}}$ signal output when the $\overline{\text{EL}}$ signal stops the LSI from generating pulses.
- To select whether an origin return initiates the $\overline{\text{CLR}}$ signal or not, set bit 2 of THE extension mode register 2 at—
  - 0: No $\overline{\text{CLR}}$ signal output at the completion of origin return
  - 1: The $\overline{\text{CLR}}$ signal output at the completion of origin return
- To select the output logic of $\overline{\text{CLR}}$ signal, set bit 3 of the extension mode register 2 at—
  - 0: Negative logic
  - 1: Positive logic

(3) ALM Signal (Forced Stop)

The LSI can input the alarm signal from the servomotor driver. It immediately stops generating pulses upon receiving the ALM signal. You can set the LSI so that it outputs the $\overline{INT}$ signal when stopping pulse output.
If the start mode command is written with the ALM signal turned on, the LSI does not generate any pulse and keeps the stop condition. The LSI starts generating pulses when the ALM signal is turned off.
The LSI can accept the ALM signal with a pulsewidth of 50nS or so. However, using the output mode command, you can turn the input filter on to cancel ALM signals with a pulsewidth of shorter than four cycles of the reference clock (approximately 800nS with a reference clock of 4.9152MHz).
The ALM signal and the SUBCLK signal use a common pin. Select the pin function as required. Also, you can change the input logic of ALM signal.

- To select the input signal of SUBCLK/ALM pin, set bit 22 of the extension mode register 2 at—
  0: SUBCLK signal for special operation
  1: ALM signal
- To select the input logic of SUBCLK/ALM pin, set bit 13 of the extension mode register at—
  0: Positive logic
  1: Negative logic
- To select whether the $\overline{INT}$ signal is output or not when the LSI stops generating pulses, set bit 5 of the start mode command at—
  0: No $\overline{INT}$ signal output at the stop and the $\overline{INT}$ signal reset
  1: $\overline{INT}$ signal output at the stop
- To check the ON/OFF status of SUBCLK/ALM signal, read bit 15 of the extension status register.
  0: ALM signal = OFF
  1: ALM signal = ON
- To check whether the factor that stopped the LSI from generating pulses is the ALM signal or not, read bit 13 of the extension status register.
  0: No
  1: ALM signal
- To turn the $\overline{ORG}$, $\overline{EL}$ and ALM signal input filter on/off, set bit 5 of the output command buffer at—
  0: OFF
  1: ON (minimum pulsewidth of four cycles of the reference clock)

5.4.2 Pulse Output Mode

By setting the output mode command, you can select either the common pulse mode or the 2-pulse mode. Using the extension mode register 1, you can change the output logic or mask the pulse output.

Select the common pulse mode. The LSI will generate pulses through the $\overline{\text{POUT}}$ pin and the direction signal through the PDIR pin. In the default negative logic, the direction signal indicates the plus direction at high level and the minus direction at low level. Notice that some motor drivers using the common pulse mode require a time to accept pulses after the direction signal is changed.

Select the 2-pulse mode. The LSI will output plus direction pulses through the $\overline{\text{POUT}}$ pin and minus direction pulses through the PDIR pin.

Settings vs. Output Signals

Mode		Common Pulse Mode		2-pulse Mode	
Logic	Direction	$\overline{\text{POUT}}$ pin	PDIR pin	$\overline{\text{POUT}}$ pin	PDIR pin
Negative	Plus		(High)		(High)
	Minus		(Low)	(High)	
Positive	Plus		(Low)		(Low)
	Minus		(High)	(Low)	

- To select the pulse output mode, set bit 1 of the output mode command at—
  0: Common pulse mode
  1: 2-pulse mode
- To select the output logic of POUT/PDIR signal, set bit 11 of the extension mode register 1 at—
  0: Negative logic
  1: Positive logic
- To select whether or not to mask output pulses, set bit 10 of the extension mode register 11 at—
  0: Pulse output
  1: Pulse masked
- To check the ON/OFF status of pulse output, read bit 7 of the extension status register.
  0: OFF
  1: ON

5.4.3 Present Position Counter (R10 Register)

The LSI provides the up/down counter for present position control. You can select the type of input signal to the counter from either the output pulse from the $\overline{\text{POUT}}$/PDIR pin or the external input pulse to the $\overline{\text{EC-A}}$/$\overline{\text{EC-B}}$ pin. You can select the counting unit (e.g. counting every five pulses). If the external input pulse is selected, you can let the counter count plus and minus pulses or 90° phase difference signals. You can also change the input logic in common with the Z-phase signal.

In the case of output pulse, the up/down counter counts when the pulse is output. In the case of external 2-pulse input, the up/down counter counts at the edge of high level (with the negative logic). In the case of 90° phase-difference signal, the up/down counter counts up when the phase of $\overline{\text{EC-A}}$ input signal advances over that of $\overline{\text{EC-B}}$ signal. The 90° phase-difference signal may be counted through 1, 2 or 4 times multiplication.

The counting range is 000000HEX to FFFFFFHEX. To reset the present position counter, write 000000HEX to the R10 register. Also, the present position counter can count up or down from a preset value.

The PCL240MS is equipped with input pins dedicated to the external signals, $\overline{\text{EC-A}}$ and $\overline{\text{EC-B}}$. With the PCL240AS, these pins are common to $\overline{\text{EXTP}}$ and INS pins, respectively.

- To turn the present position counter on or off, set bit 5 of the control mode command at—
  0: OFF
  1: ON
- To set the counting unit of present position counter, use bits 3 to 0 of the extension mode register 1. The setting range availabhle is 0000 to 1111 (0 to 15). The counting unit is a set value + 1. If you set at 0, the counter counts every one pulse. If you set at 15, the counter counts every 16 pulses.
- To select the type of input signal to the present position counter, set bit 7 of the extension mode register 1 at—
  0: Output pulse from $\overline{\text{POUT}}$/PDIR pin
  1: Input pulse to $\overline{\text{EC-A}}$/$\overline{\text{EC-B}}$ pin
- To select the external input mode, set bit 6 of the extension mode register at—
  0: Plus/minus pulse
  1: 90° phase difference signal

- To multiply the 90° phase difference signal for counting, set bits 5 and 4 at:
  00 or 01: 1 time
  10: 2 times
  11: 4 times
- To select the external input logic of present position counter, set bit 12 of the extension mode register at—
  0: Negative logic
  1: Positive logic
  The selected logic is commonly used for the $\overline{\text{EC-Z}}$ signal.

5.4.4 External Mechanical Signals

As position detection signals, the LSI can input the following five signals from the external mechanical system.

(1) $\overline{\text{EL+}}$ and $\overline{\text{EL–}}$ Signals

The end limit signal in the moving direction (e.g. $\overline{\text{EL+}}$ signal when the LSI is generating plus direction pulses) immediately stops the LSI from generating pulses and lets it keep the suspended condition even if the signal is turned off. You can let the LSI output the $\overline{\text{INT}}$ signal when stopping pulse output.

If the start mode command is written with the end limit signal ON, the LSI does not generate any pulse, keeping the suspended condition. When the $\overline{\text{EL}}$ signal is turned off, the LSI starts generating pulses..

The LSI can accept $\overline{\text{EL}}$ signals with a pulsewidth of 50nS or so. But you can cancel $\overline{\text{EL}}$ signals with a pulsewidth of shorter than four cycles of the reference clock (approximately 800nS with a reference clock of 4.9152MHz) by turning the input filter on with the output mode command.

You can check the ON/OFF status of the signal by reading the extension status register but cannot change the input logic.

- To select whether or not to output the $\overline{\text{INT}}$ signal at the stop of pulse output, set bit 5 of the start mode command at—
  0: No $\overline{\text{INT}}$ signal output at the stop and $\overline{\text{INT}}$ reset
  1: $\overline{\text{INT}}$ signal output at the stop
- To turn the $\overline{\text{ORG}}$, $\overline{\text{EL}}$ and ALM signal input filter on or off, set bit 5 of the output mode command at—
  0: OFF
  1: ON (minimum pulsewidth: four cycles of the reference clock)
- To check the ON/OFF status of $\overline{\text{EL+}}$ pin, read bit 1 of the status buffer.
  0: OFF
  1: ON

- To check the ON/OFF status of $\overline{EL-}$ signal, read bit 0 of the status buffer.
- To check whether the factor that stopped the LSI from generating pulses is the $\overline{EL+}$ signal or not, read bit 9 of the extension status register.
  0: No
  1: Yes, $\overline{EL+}$ signal
- To check whether the factor that stopped the LSI from generating pulses is the EL− signal or not, read bit 8 of the extension mode register.
  0: No
  1: Yes, $\overline{EL-}$

(2) $\overline{SD+}$ and $\overline{SD-}$ Signals

During varied-speed operation, the ramping-down signal in the moving direction lets the LSI decelerate to the FL rate. If the signal is turned off during or after deceleration, the output pulse rate is accelerated to the FH rate. If the start mode command for varied-speed operation is written with the $\overline{SD}$ signal ON, the LSI keeps generating pulses at the FL rate without accelerating to the FH rate.
You can make the SD signal control valid or invalid using the control mode command and check the signal status by reading the extension status register.
Using $\overline{SD}$ signals, you can perform Z-phase signal counting origin return through deceleration. Refer to "5.3.3 Origin Return."

- To make the $\overline{SD}$ signal control valid or invalid, set bit 1 of the control mode command at—
  0: $\overline{SD\pm}$ signal control invalid
  1: $\overline{SD\pm}$ signal control valid
- To check the ON/OFF status of $\overline{SD+}$ signal, read bit 3 of the extension status register.
  0: $\overline{SD+}$ signal = OFF
  1: SD+ signal = ON
- To check the ON/OFF status of $\overline{SD-}$ signal, read bit 2 of the extension status register.
  0: $\overline{SD-}$ signal = OFF
  1: SD− signal = ON

(3) $\overline{ORG}$ Signal

Use the $\overline{ORG}$ signal for origin return (refer to "5.3.3 Origin Return").
If you use the $\overline{ORG}$ signal only to stop the LSI from generating pulses, the LSI can accept the signal with a pulsewidth of 50nS or so. However, you can cancel $\overline{ORG}$ signals with a pulsewidth of shorter than four cycles of the reference clock (approximately 800nS with a reference clock of 4.9152MHz) by turning the input filter ON with the output mode command.
You can make the signal valid or invalid with the control mode command and check the ON/OFF status by reading the status buffer.

You can also perform origin return by using the $\overline{\text{ORG}}$ signal in combination with the Z-phase signal. To stop the LSI from generating pulses after the preset number of Z-phase signals, keep the $\overline{\text{ORG}}$ signal as turned on until the LSI stops generating pulses. The input logic can be changed. The Z-phase signal input pin is the $\overline{\text{EC-Z}}$ pin.

- To make the $\overline{\text{ORG}}$ signal control valid or invalid, set bit 0 of the control mode command at—
  0: $\overline{\text{ORG}}$ signal control invalid
  1: $\overline{\text{ORG}}$ signal control valid
- To check the ON/OFF status of $\overline{\text{ORG}}$ signal, read bit 2 of the status buffer.
  0: $\overline{\text{ORG}}$ signal = OFF
  1: $\overline{\text{ORG}}$ signal = ON
- To change the input logic of $\overline{\text{ORG}}$ signal, set bit 23 of the extension mode register at—
  0: Negative logic
  1: Positive logic
- To turn the $\overline{\text{ORG}}$, $\overline{\text{EL}}$ and ALM signal input filter on or off, set bit 5 of the output mode command at—
  0: OFF
  1: ON (minimum pulsewidth of four cycles of reference clock)
- To select the condition to complete an origin return, set bit 21 of the extension mode register at—
  0: No $\overline{\text{EC-Z}}$ signal used ($\overline{\text{ORG}}$ signal only)
  1: Z-phase signal counted
- To select the timing to start counting Z-phase signals, set bit 20 of the extension mode register at—
  0: After $\overline{\text{SD}}$ signal is turned on
  1: After $\overline{\text{ORG}}$ signal is turned on
- To select the number of Z-phase signals counted, set bits 19 to 16 at (counting number − 1). The setting range is 0 to 15.
- To check the Z-phase signal counter for origin return, read bits 19 to 16 of the extension status register.
- To change the input logic of $\overline{\text{EC-Z}}$ signal, set bit 12 of the extension mode register at—
  0: Negative logic
  1: Positive logic
  The selected logic is commonly used as the external input logic for the present position counter.

- To check the ON/OFF status of $\overline{\text{EC-Z}}$ signal, read bit 20 of the extension mode register.
  0: $\overline{\text{EC-Z}}$ signal = OFF
  1: EC-Z signal = ON
- To select whether or not to output the $\overline{\text{INT}}$ signal when the LSI stops generating pulses, set bit 5 of the start mode command at—
  0: No $\overline{\text{INT}}$ signal output at the stop ($\overline{\text{INT}}$ signal reset)
  1: $\overline{\text{INT}}$ signal output at the stop
- To check whether the $\overline{\text{ORG}}$ signal stopped the LSI from generating pulses or not, read bit 10 of the extension mode register.
  0: No
  1: $\overline{\text{ORG}}$ signal ($\overline{\text{SD}}$ signal + $\overline{\text{EC-Z}}$ signals counted) stopped the LSI.

5.4.5 General-purpose Input/Output Pins

The LSI provides the OTS pin for general-purpose output and the INS pin for general-purpose input. Note, however, that the $\overline{\text{SYN1}}/\overline{\text{INP}}$ pin and the INS pin use the same status bit and, therefore, if you monitor the $\overline{\text{SYN1}}/\overline{\text{INP}}$ pin, you cannot use the INS pin. Also, in the case of PCL240AS, the INS pin is common to the EC-A pin and, therefore, if you select external input for the present position counter, you cannot use the INS pin.

- To select the level of general-purpose output pin OTS, set bit 3 of the register select command at—
  0: OTS pin = Low level
  1: OTS pin = High level
- To select the monitoring pin, the INS pin or the $\overline{\text{INP}}$ pin, set bit 14 of the extension mode register at—
  0: INS pin monitored
  1: $\overline{\text{INP}}$ pin/$\overline{\text{SYN1}}$ pin monitored
- To check the level of general-purpose input pin INS (with the pin selected for monitoring), read bit 4 of the status buffer.
  0: INS pin = Low level
  1: INS pin = High level

5.4.6 Interrupt Signal Output

The LSI can output an interrupt signal to the CPU at the time it stops generating pulses and at the ramping-down point. You can check the ON/OFF status by reading the status buffer and if both factors are made valid, you can check which factor causes the interrupt signal by reading the extension status register.
Furthermore, if the interrupt signal is generated at the stop, you can check the factor which stopped the LSI by reading the extension status register.

By setting the $\overline{INT}$ signal output control bit at 0, you can reset the $\overline{INT}$ signal to high level.
If you use two or more units, you can connect their $\overline{INT}$ pins in WIRED OR. In such a case, however, you need to connect an external pull-up resistor of 5kΩ to 10kΩ.

- To select whether or not to output the $\overline{INT}$ signal at the stop, set bit 5 of the status mode register at:
  0: No $\overline{INT}$ signal output at the stop and $\overline{INT}$ signal reset
  1: $\overline{INT}$ signal output at the stop
- To select whether or not to output the $\overline{INT}$ signal at the ramping-down point, set bit 13 of the extension mode register 1 at—
  0: No $\overline{INT}$ signal output at the ramping-down point and $\overline{INT}$ signal reset
  1: $\overline{INT}$ signal output at the ramping-down point
- To check the ON/OFF status of $\overline{INT}$ signal, read bit 7 of the status buffer.
  0: $\overline{INT}$ signal = ON
  1: $\overline{INT}$ signal = OFF
- To check the interrupt signal ON/OFF status at the stop, read bit 0 of the extension status register.
  0: $\overline{INT}$ signal at the stop = ON
  1: INT signal at the stop = OFF
- To check the factor which stopped the LSI from generating pulses, read bits 14 to 8 of the extension status register.
  Bit 8 = 1: Stop due to $\overline{EL-}$ signal
  Bit 9 = 1: Stop due to $\overline{EL+}$ signal
  Bit 10 = 1: Stop due to $\overline{ORG}$ signal
  Bit 11 = 1: Stop due to completion of preset mode operation
  Bit 12 = 1: Stop due to deceleration-stop command
  Bit 13 = 1: Stop due to ALM signal
  Bit 14 = 1: Stop due to stop command
  = 0: No stop factor

5.5 Registers

To write or read data to/from a register, you need to select in advance the register with the register select command. If the data are read as 24-bit data, 0 is put in all high-place bits which are not used. In the interchangeable mode with the 240K, registers R10 to R17 cannot be used. For calculation formulas concerning registers, refer to "5.1 Pulse Output Pattern."

Register No.	Function	Setting Range	Bit Length
R0	Preset counter	0 to 16,777,215 (FFFFFF)	24
R1	FL pulse rate setting	1 to 8,191 (1FFF)	13
R2	FH1 pulse rate setting	1 to 8,191 (1FFF)	13
R3	FH2 pulse rate setting	1 to 8,191 (1FFF)	13
R4	Acceleration rate setting	2 to 65,535 (FFFF)	16
R5	Deceleration rate setting	2 to 65,535 (FFFF)	16
R6	Ramping-down point setting	0 to 16,777,215 (FFFFFF)	24
R7	Multiplication factor setting	2 to 65,535 (FFFF)	16
R10	Present position counter	0 to 16,777,215 (FFFFFF)	24
R11	Present pulse rate monitor	1 to 8,191 (1FFF)	13
R12	Extension mode 1 setting		24
R13	Extension mode 2 setting		24
R14	S-curve accel. section setting	0 to 4,095 & control bit 1	16
R15	S-curve decel. section setting	0 to 4,095 (FFF)	12
R16	Command buffer monitor		24
R17	Extension status		21

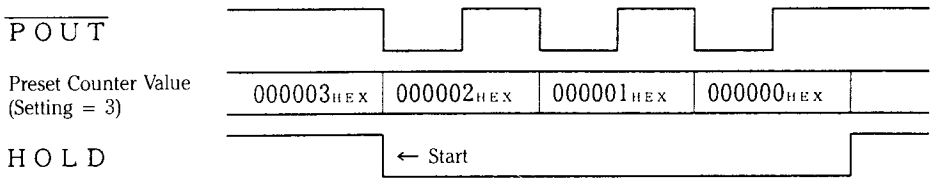
5.5.1 R0—Preset Counter Setting Register, 24-bit

The LSI has the built-in down counter which is set at the value (number of output pulses) written to the R0 register. The setting/counting range is 0 to 16,777,215 ($FFFFFF_{HEX}$). For preset mode operation, the down counter should be set at 1 or higher value. In any operation mode, the preset counter counts down at every one pulse output. If you let it count down from 0, the counter is set at a maximum value ($FFFFFF_{HEX}$). If the $\overline{EXTP}$ signal is selected as the counter input in the output mode command, the preset counter counts down at every one pulse input to the $\overline{EXTP}$ pin.

You can read the counter value (remaining number of output pulses) whether pulse output is in progress or in cessation. To read the counter value during pulse output in progress, it is recommended to read all 24 bits collectively so as to avoid erroneous reading. Write the R0 select command every time you read all 24 bits collectively, since the data are latched in the 24-bit reading buffer at the time the register select command is written.

For the preset mode operation, enter the number of output pulses in the R0 register and then start the LSI generating pulses. The preset counter will count down the value and when it counts down to 0 (the LSI completes outputting pulses to the preset number), the LSI will stop generating pulses. Write the $\overline{CLR}$ command after the stop.
If a command or an external signal suspends pulse output in the preset mode, the preset counter keeps the remaining number of output pulses, thereby letting the next start mode command start the LSI generating pulses to the remaining number. After counting down to 0, the preset counter keeps 0. Therefore, if the same number of output pulses is used, you need to set the R0 register anew.

Operation of Preset Counter



- To select the type of input signal to the preset counter, set bit 2 of the output mode command at—
  0: Counting output pulses from the $\overline{POUT}$/PDIR pin
  1: Counting input signals to the $\overline{EXTP}$ pin
- To select the register read/write method, set bit 5 of the register select command at—
  0: Every 8 bits
  1: All 24 bits in a lump

5.5.2 R1—FL Pulse Rate Setting Register, 13-bit

In varied-speed operation, the LSI starts generating pulses at the FL pulse rate and then accelerates to the FH pulse rate. Writing the deceleration-stop command thereafter lets the LSI stop generating pulses after decelerating the output to the FL pulse rate.
The output pulse rate is; R1 value x value in R7 register. The setting range of R1 register is 1 to 8,191 (1FFFHEX). If you use the previous setting value, you need not write anew.
If you set the FL pulse rate at 0, the $\overline{POUT}$ pin will be locked to low level at the end and the LSI may not stop generating pulses. Therefore, be sure to set the FL pulse rate at 1 or higher.

5.5.3 R2—FH1 Pulse Rate Setting Register, 13-bit

For varied-speed operation, set the R2 register at a higher value than what is written to the R1 register. The output FH1 pulse rate is; (R2 value) x (value in the R7 register). The setting range of R2 register is 1 to 8,191 ($1FFF_{HEX}$). If you use the previous setting value, you need not write anew.

5.5.4 R3—FH2 Pulse Rate Setting Register, 13-bit

For varied-speed operation, set the R3 register at a higher value than what is written to the R1 register. The output FH2 pulse rate is; (R3 value) x (value in the R7 register). The setting range of R3 register is 1 to 8,191 ($1FFF_{HEX}$). If you use the previous setting value, you need not write anew.
You may use either FH1 or FH2 pulse rate for varied-speed operation. Also, you can switch from one to another during pulse output in progress.

5.5.5 R4—Acceleration Rate Setting Register, 16-bit

The R4 register sets the acceleration rate for varied-speed operation. If the automatic ramping-down point setting function is used, the rate determined by the R4 register is applied to deceleration as well.
The setting range is 2 to 65,535 ($FFFF_{HEX}$). If you use the previous setting value, you need not write anew.

5.5.6 R5—Deceleration Rate Setting Register, 16-bit

The R5 register sets the deceleration rate which will be used if the automatic ramping-down point setting function is made invalid. The setting range is 2 to 65,535 ($FFFF_{HEX}$). If you use the previous setting value, you need not write anew.

5.5.7 R6—Ramping-down Point Setting Register, 24-bit

The R6 register sets the starting point of deceleration for varied-speed operation in the preset mode. The LSI will decelerate when the preset counter R0 counts down to a value equal to or lower than the R6 value. If the start mode command is written with R6 $\geqq$ R0, at the beginning, the LSI does not accelerate and keeps generating pulses at the FL rate.
The setting range is 1 to 16,777,215 ($FFFFFF_{HEX}$). If the automatic ramping-point setting function is made valid, the R6 value is offset from the automatic setting value, thereby making the set range $-8,388,608$ (800000_{HEX}) to $+8,388,608$ ($7FFFFF_{HEX}$). In this case, the set value is reset by the $\overline{CLR}$ command.

When the automatic ramping-down point setting is valid, set the R6 register at 0 except for the case you shift the starting point of deceleration. Refer to "5.1.10 Ramping-down Point Setting."

5.5.8 R7—Multiplication Factor Setting Register, 16-bit

The R7 register sets the factor to multiply R1, R2 and R3 values in a range of 2 to 65,535 (FFFF$_{HEX}$). The smaller the R7 value, the higher the output clock frequency. If you use the previous setting value, you need not write anew. Refer to "5.1.1 Setting Multiplication Factor."

The following registers R10 to R17 are usable only in the standard mode initiated by setting bit 3 of the output mode command at 1.

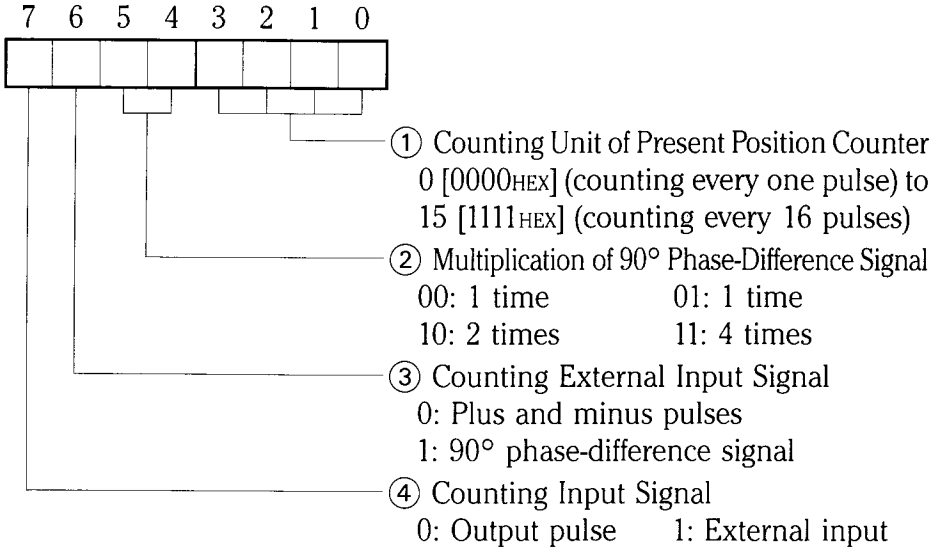
5.5.9 R10—Present Position Counter, 24-bit

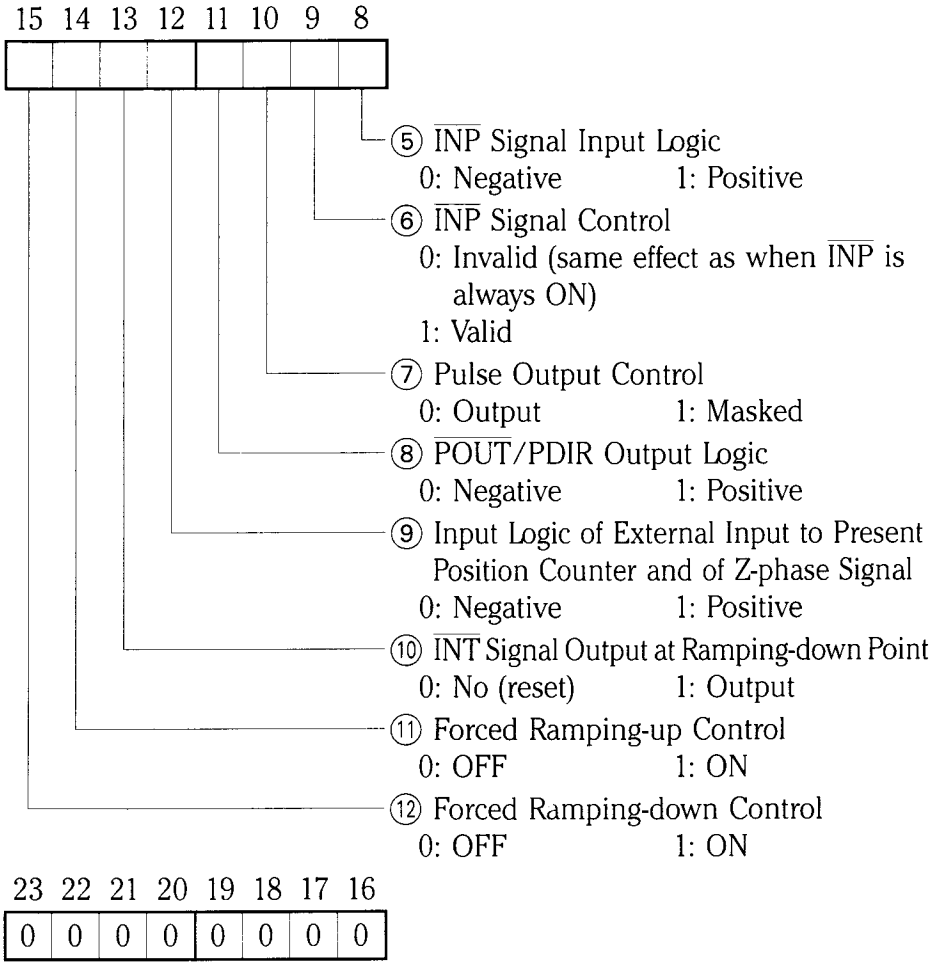
This 24-bit binary up/down counter can be used to control the present position. You can select the type of input signal to the counter from either output pulse or external input signal. You can also select the counting unit in a range of 1 to 16 pulses per count. The setting/counting range is 0 to 16,777,215 (FFFFFF$_{HEX}$). Refer to "5.4.3 Present Position Counter."

5.5.10 R11—Present Pulse Rate Monitor, 13-bit

This read-only register allows you to monitor the present pulse rate. Note, however, that the value monitored is what is written in the R1, R2 or R3 register and not the output pulse rate (R1, R2 or R3 x multiplication factor). During pulse output in cessation, the monitored value is same as the value written to the R1 register (FL rate).

5.5.11 R12—Extension Mode Register 1, 24-bit





Setting:

① Counting Unit of Present Position Counter (Bits 3 to 0)

You can set the counting unit of present position counter in a range of 0 (0000HEX) to 15 (1111HEX). The present position counts every (set value + 1) pulses. (e.g. it counts every 12 pulses if the counting unit is set at 11 (1011HEX).

② Multiplication of External 90° Phase Difference Signal to Present Position Counter (Bits 5 and 4)

When controlling the present position using 90° phase difference signals of encoder, you can multiply the signals to input them to the present position counter. The present position counter counts up when the phase of $\overline{\text{EC-A}}$ signal advances over that of the $\overline{\text{EC-B}}$ signal.

③ Type of External Signals Input to Present Position Counter (Bit 6)

When letting the present position counter count external input signals, you can select plus and minus pulses or 90° phase difference signals. In the case of plus and minus pulses with the negative logic, it counts at the rising edge.

④ Type of Input Signal to Present Position Counter (Bit 7)

You can select the type of input signal to the present position counter from output pulse and external input signal.

⑤ $\overline{\text{INP}}$ Signal Input Logic (Bit 8)

You can select the $\overline{\text{INP}}$ signal input logic when using the $\overline{\text{SYN1}}/\overline{\text{INP}}$ pin for $\overline{\text{INP}}$ signal input.

⑥ $\overline{\text{INT}}$ Signal Control (Bit 9)

You can select "1" when using $\overline{\text{SYN1}}/\overline{\text{INP}}$ pin for $\overline{\text{INP}}$ signal input.

⑦ Pulse Output Control (Bit 10)

You can mask the pulse output from the $\overline{\text{POUT}}$/PDIR pin. If the pulse output is masked, the preset counter and present position counter continue counting internal pulses. $\overline{\text{EL}}$, $\overline{\text{ORG}}$ and ALM signals have no function when the pulse output is masked.

⑧ Output Logic of $\overline{\text{POUT}}$ and PDIR Pins (Bit 11)

You can select the output logic of $\overline{\text{POUT}}$ and PDIR pins. Refer to "5.4.2 Pulse Output Mode."

⑨ Present Counter External Input & Z-phase Signal Logic (Bit 12)

You can set the input logic of $\overline{\text{EC-A}}$, $\overline{\text{EC-B}}$ and $\overline{\text{EC-Z}}$ signals.

⑩ $\overline{\text{INT}}$ Signal Output at Ramping-down Point (Bit 13)

You can select whether or not to output the $\overline{\text{INT}}$ signal when the preset counter counts down to a value lower than the ramping-doint point. You can reset the signal by setting bit 13 at 0.

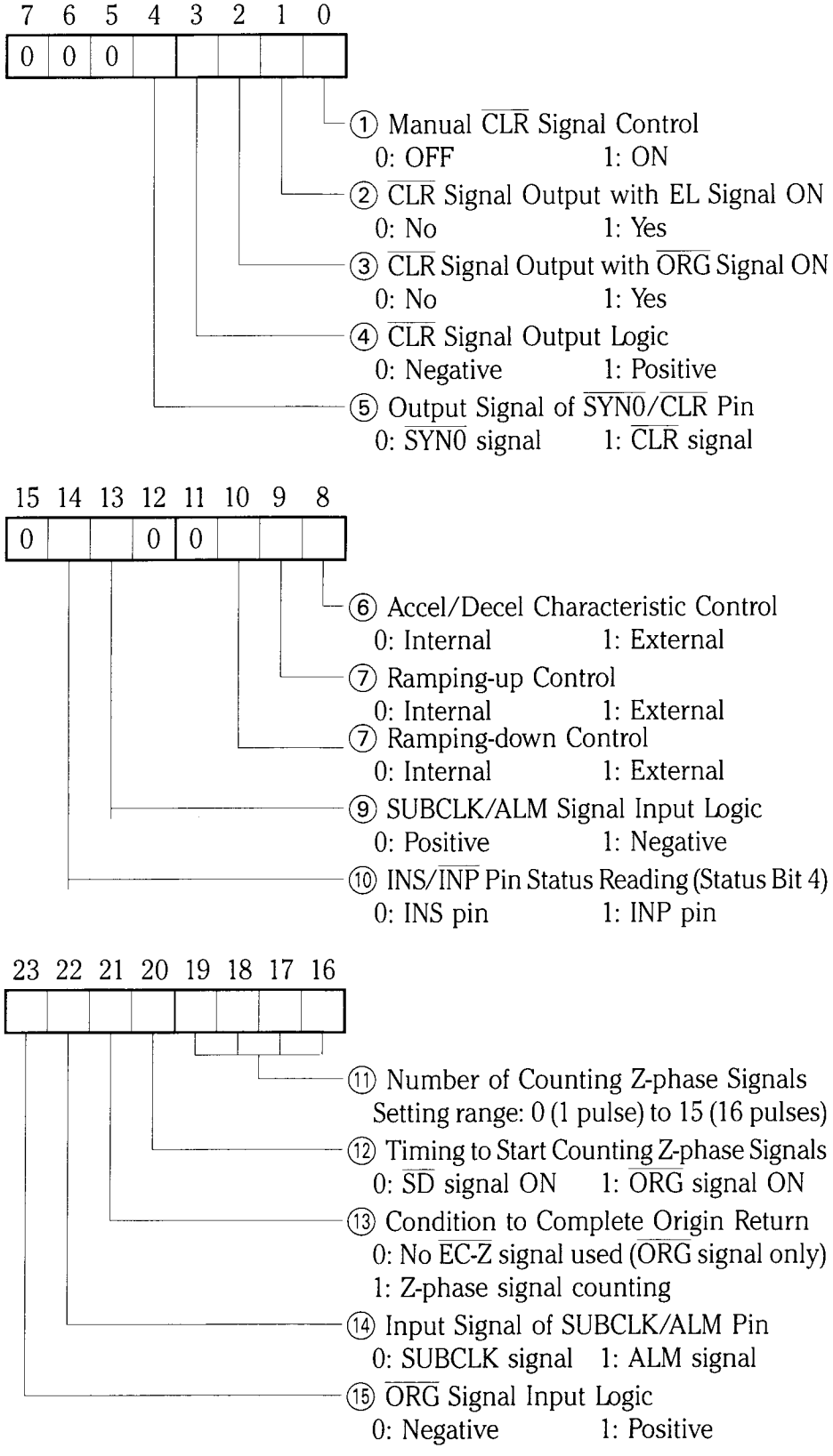
⑪, ⑫ Forced Ramping-up Control (Bit 14) and Forced Ramping-down Control (Bit 15)

By turning the forced ramping-up control on, you can accelerate the pulse output from the present pulse rate to a maximum pulse rate (8191 x multiplication factor) at the set acceleration rate.

Similarly, by turning the forced ramping-down control on, you can decelerate the pulse output from the present pulse rate to a minimum pulse rate (0) at the set deceleration rate. Do not use the forced ramping-up and the forced ramping-down at a time. If the ramping-up/down control is turned off during ramping-up/down in progress, the LSI keeps generating pulses at the pulse rate used at that time.

To use the forced ramping-up/down control, set bit 4 of the output mode command at 1 to turn the ramping-up/down control OFF. Note that forced ramping-up/down is performed in linear profile.

5.5.12 R13—Extension Mode Register 2, 24-bit



Setting:

① Manual $\overline{CLR}$ Signal Control (Bit 0)

If the $\overline{SYN0}/\overline{CLR}$ pin is defined as the $\overline{CLR}$ signal output pin, you can manually control the $\overline{CLR}$ signal output by setting bit 0 at 1.

② $\overline{CLR}$ Signal Output with $\overline{EL}$ Signal (Bit 1)

If the $\overline{SYN0}/\overline{CLR}$ pin is defined as the $\overline{CLR}$ signal output pin and bit 1 of the extension mode register 2 is set at 1, the LSI will output the $\overline{CLR}$ signal with a pulsewidth of 8 cycles of reference clock when the $\overline{EL}$ signal is turned on.

③ $\overline{CLR}$ Signal Output with $\overline{ORG}$ Signal (Bit 2)

If the $\overline{SYN0}/\overline{CLR}$ pin is defined as the $\overline{CLR}$ signal output pin and bit 2 of the extension mode register 2 is set at 1, the LSI will output the $\overline{CLR}$ signal with a pulsewidth of 8 cycles of reference clock when the $\overline{ORG}$ signal is turned on.

④ $\overline{CLR}$ Signal Output Logic (Bit 3)

If the $\overline{SYN0}/\overline{CLR}$ pin is defined as the $\overline{CLR}$ signal output pin, you can select the $\overline{CLR}$ signal output logic by setting this bit.

⑤ Output Signal of $\overline{SYN0}/\overline{CLR}$ Pin (Bit 4)

You can select which signal is output from the $\overline{SYN0}/\overline{CLR}$ pin, Refer to "5.4.1 Servomotor Interface, (2) $\overline{CLR}$."

⑥ Acceleration/Deceleration Characteristic Control

You can select which control clock is used for the acceleration/deceleration control circuit, the reference clock or the clock from the SUBCLK pin. The SUBCLK pin was intended for the PCL-240AK/PCL-240MK to input frequency-varied clock for S-curve acceleration/deceleration. With the PCL240AS/PCL240MS, you can perform S-curve acceleration/deceleration without using the external clock signal. If the external control is selected, the internal S-curve control circuit is disconnected and, therefore, inputting a frequency-constant SUBCLK signal results in linear acceleration/deceleration.

⑦, ⑧ Ramping-up Control (Bit 9) and Ramping-down Control (Bit 10)

The LSI controls acceleration and deceleration according to the parameters written to the acceleration rate setting register R4 and the deceleration rate setting register R5. You can switch the mode from the internal control to the external control. Under the external control, acceleration/deceleration is made step by step at every one clock input to the SUBCLK pin. The chip discards any clock input after the maxiumum pulse rate (8191 x multiplication factor) or the minimum pulse rate (0) is reached.

⑨ Input Logic of SUBCLK/ALM Signal (Bit 13)

You can make the input logic of SUBCLK/ALM signal positive or negative.

⑩ INS/$\overline{\text{INP}}$ Pin Status Reading (Bit 14

You can select which pin is monitored at status bit 4, INS pin or SYN1/$\overline{\text{INP}}$ pin.

⑪ Number of Counting Z-phase Signals (Bits 19 to 16)

When you perform an origin return with the Z-phase signal counting method, set the number of counting Z-phase signals which completes the origin return. The setting range is 0 (0000_{BIN}) to 15 (1111_{BIN}). The counting number is (set value + 1). If you set these bits at 11 (1011_{BIN}), the 12th $\overline{\text{EC-Z}}$ pulse signal after the $\overline{\text{ORG}}$ signal is turned on stops the chip from generating pulses.

⑫ Timing to Start Counting Z-phase Signals (Bit 20)

When you perform an origin return with the Z-phase signal counting method, select which signal is used for the origin return, $\overline{\text{ORG}}$ signal or $\overline{\text{SD}}$ signal.

⑬ Condition to Complete Origin Return (Bit 21)

When you perform an origin return, select the condition to complete the origin return, $\overline{\text{ORG}}$ signal only or $\overline{\text{ORG}}$ signal (or $\overline{\text{EL}}$ signal) plus Z-phase signals from the $\overline{\text{EC-Z}}$ pin. Refer to "5.3.3 Origin Return."

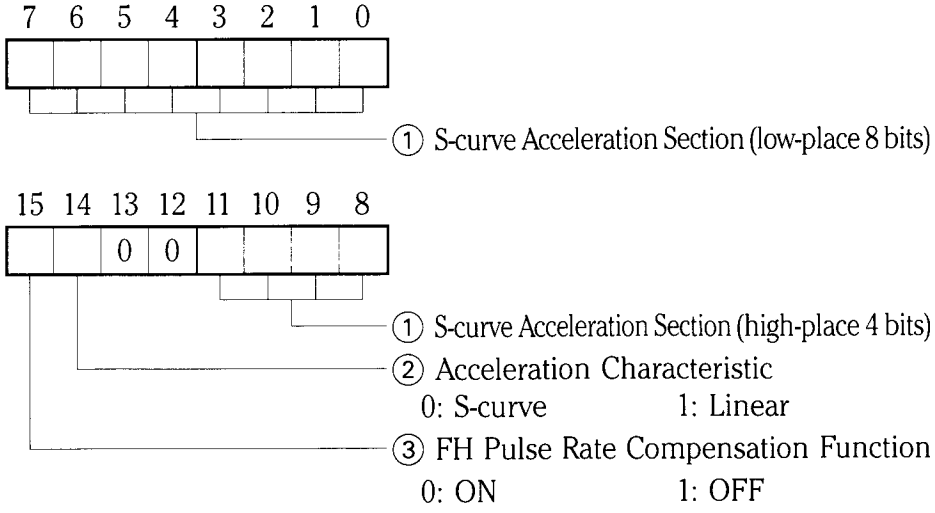
⑭ Input Signal of SUBCLK/ALM Pin (Bit 22)

Set the bit at 1 to use the pin as the ALM pin.

⑮ $\overline{\text{ORG}}$ Signal Input Logic (Bit 23)

You can make the $\overline{\text{ORG}}$ signal input logic positive or negative.

5.5.13 R14—S-curve Acceleration Section Setting Register, 16-bit



① S-curve Acceleration Section (Bits 11 to 0)

Obtain the value to be written to these bits by dividing a desired S-curve acceleration section in pps by multiplication factors. For details, refer to "5.1 Pulse Output Pattern."

② Acceleration/Deceleration Characteristic (Bit 14)

You can select S-curve or linear acceleration/deceleration. If linear is selected, the acceleration/deceleration time is the same as the time of the S-curve acceleration/deceleration with no linear section.

③ FH Pulse Rate Compensation Function (Bit 15)

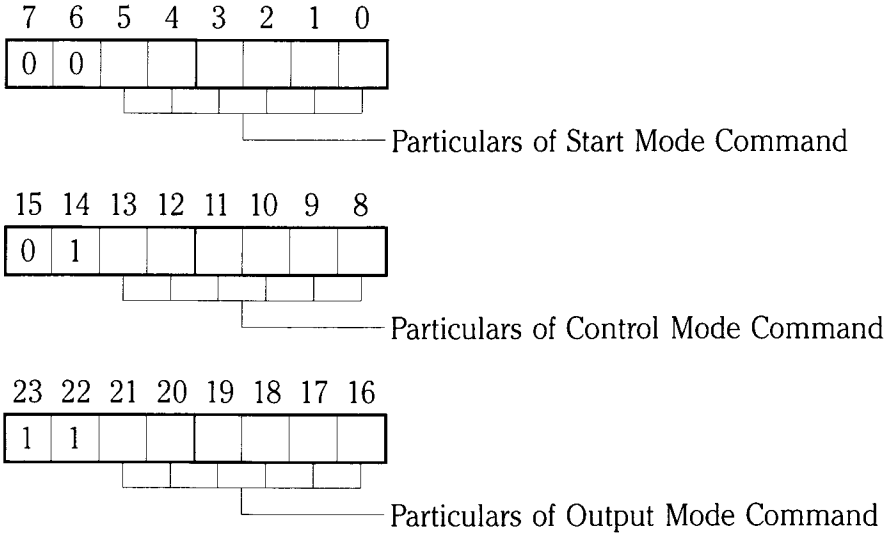
If the number of pulses is too small for varied-speed operation in preset mode, the FH pulse rate compensation function automatically decreases the FH pulse rate to avoid a triangular motion. Note, however, that parameters written in R2 and R3 registers do not change. If a triangular motion is acceptable, set this bit at 1. The compensation function will be made invalid, thereby reducing the moving time. Refer to "5.1 Pulse Output Pattern."

5.5.14 R15—S-curve Deceleration Section Setting Register, 12-bit

Refer to "5.1 Pulse Output Pattern."

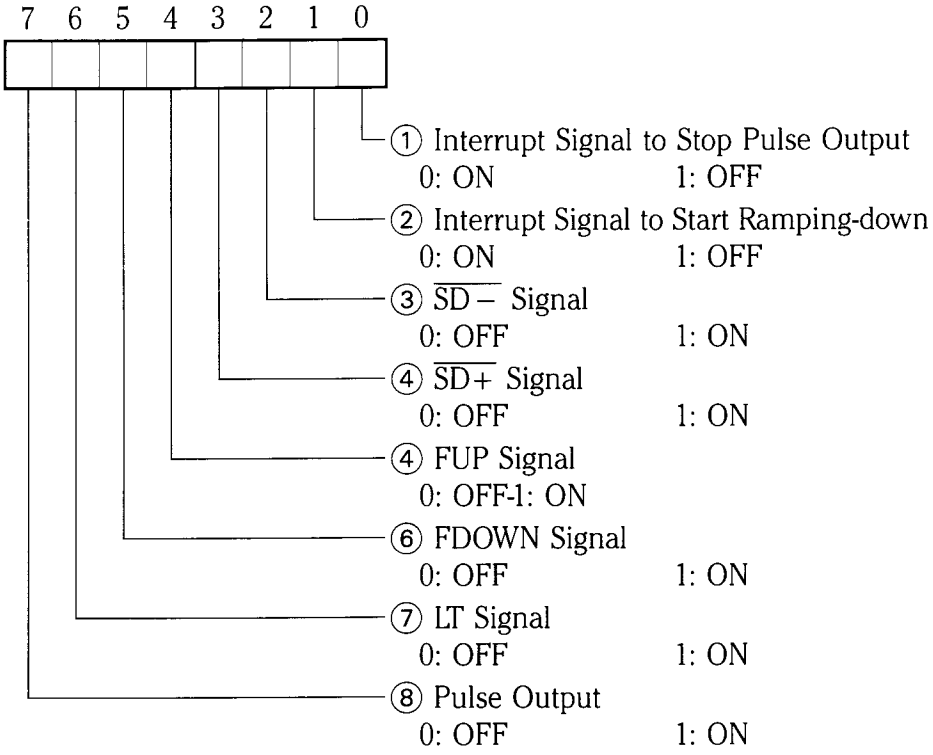
5.5.15 R16—Command Buffer Monitor, 24-bit

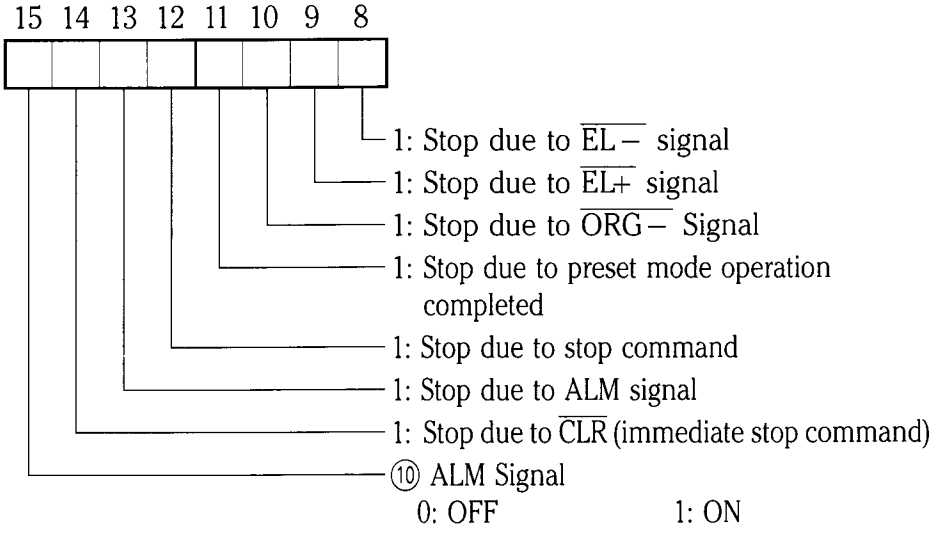
You can check the particulars written to the command buffer. Note, however, that you cannot read the register select command.

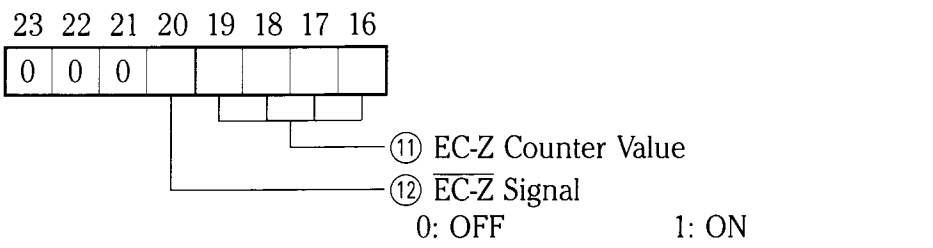


5.5.16 R17—Extension Status Monitor, 21-bits

Through the R17 register, you can monitor pin status, stop factors, Z-phase signal counting, etc.







Setting:

①, ② Interrupt Signal to Stop Pulse Output (Bit 0) and Interrupt Signal to Start Ramping-down (Bit 1)

If both interrupt factors are made valid, you have to check which signal caused the interupt.

③ ~ ⑦ ON/OFF Status of $\overline{SD\pm}$ (Bits 3 and 2), FUP (Bit 4), FDOWN (Bit 5) and LT Signal (Bit 6)

You can check the ON/OFF status of these signals. You can read the $\overline{SD\pm}$ signals even if the $\overline{SD\pm}$ singal controls are made invalid.

⑧ Pulse Output (Bit 7)

You can check the ON/OFF status of pulse output irrespective of direction, output mode and logic settings.

⑨ Stop Factors (Bits 14 to 8)

Signals at the time the LSI stopped generating pulses are latched to bits 14 to 8. By checking these bits, you can judge which factor stopped the LSI from generating pulses. The latched contents will not change until the next stop.

Bit 14 inidicates 1 when the clear command (immediate stop command, 08_{HEX}) stops the LSI from generating pulses. Bit 12 indicates 1 when the immediate stop command or deceleration-stop command ($1F_{HEX}$) stops the LSI from generating pulses. To judge which factor stopped the LSI, check the status of bit 14.

⑯ ALM Signal (Bit 15)

According to the input logic set by bit 13 of the extension mode register 2 (R13), you can check the ON/OFF status of ALM signal.

⑰ EC-Z Counter Value (Bits 19 to 16)

You can check the EC-Z counter value for origin return. Usually, the counter value is as set by bits 19 to 16 of the extension mode register 2. When the $\overline{SD}$ or $\overline{ORG}$ signal (selected by bit 20 of R13) is turned on, each $\overline{EC\text{-}Z}$ signal lets the counter count down. When it counts down to 0, the next $\overline{EC\text{-}Z}$ signal stops the LSI from generating pulses, thereby completing origin return. After then, the counter is reset to the value set by bits 19 to 16 of the extension mode register 2 (R13).

⑫ $\overline{EC\text{-}Z}$ Signal (Bit 20)

According to the input logic set by bit 12 of the extension mode register 1 (R12), you can check the ON/OFF status of $\overline{EC\text{-}Z}$ signal.

5.6 Monitor

You can monitor the following:

(1) Status Buffer and Extension Mode Register R17

Operating Status: Pulse output in cessation, accelerating, pulse output in constant-speed mode, decelerating, interrupt signal, pulse output in progress and EC-Z counter

Signals: $\overline{EL\pm}$, $\overline{ORG}$, ZERO, INS/$\overline{INP}$, FKEEP, $\overline{HOLD}$, $\overline{INT}$, $\overline{SD\pm}$, FUP, FDOWN, LT, ALM and $\overline{EC\text{-}Z}$

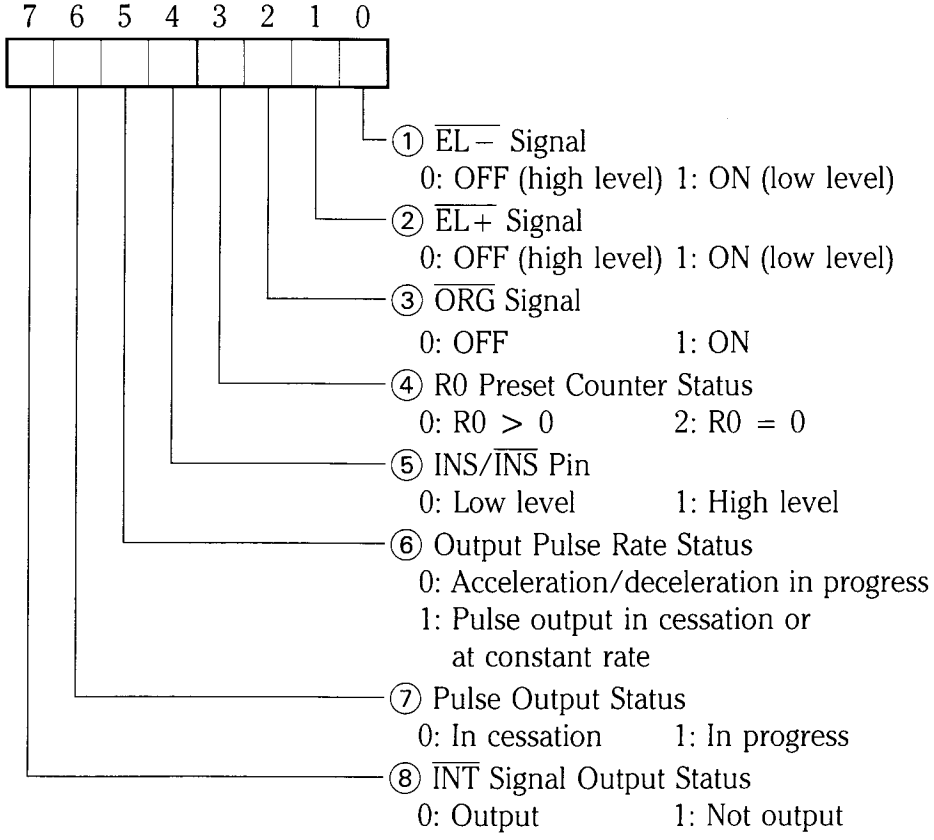
Stop factors: $\overline{EL\pm}$, $\overline{ORG}$, ALM, preset mode operation completed, stop command

(2) Registers R0 to R17

In the standard mode, you can monitor data on all registers R0 to R17. However, in the interchangeable mode with the 240K version, you can read data only from the R0 register.

5.6.1 Status Buffer

You can read external and internal signals from the status buffer. The status buffer uses the same addresses as the command buffer. If bit 5 of the register select command is set at 1, The data are once latched at the time the RD signal changes from high to low level and then are read. If bit 5 of the register select command is set at 0, the data are not latched and, therefore, the data may change during the read cycle.



①~③, ⑤ $\overline{EL-}$ (Bit 0), $\overline{EL+}$ (Bit 1), $\overline{ORG}$ (Bit 2) and INS/$\overline{INP}$ (Bit 5) Pin Status

By reading these bits, you can monitor the status of these pins; $\overline{ORG}$ signal ON/OFF based on the set input logic and SYN1/$\overline{INP}$ high/low level based on the default logic. To switch between the INS or SYN1/$\overline{INP}$ for monitoring, set bit 14 of the R13 register.

④, ⑥, ⑦ R0 Preset Counter (Bit 3), Output Pulse Rate (Bit 5) and Pulse Output Status (Bit 6)

These bits indicate the same status as the following pins:

Bit 3 (R0 preset counter status) = ZERO output pin

Bit 4 (output pulse rate status) = FKEEP output pin

Bit 6 (pulse output status) = Reversed HOLD output pin status

⑧ $\overline{INT}$ Signal Output Status

The status of bit 7 ($\overline{INT}$ signal output status) is the same as the $\overline{INT}$ output pin.

6. Hardware

6.1 Terminal Pin Assignment

[Pin No.: MS=240MS, AS=240AS]

Pin No.		Name	I/O	Logic	Description
MS	AS				
1	1	OTS	O	Positive	General-purpose output signal
2	2	CLOCK	I		Reference clock
—	2	GND	I		Ground
3	4	$\overline{\text{RESET}}$	I	Negative	Internal reset signal
4	5	A1	I	Positive	Address bus signal 1
5	6	$\overline{\text{CS}}$	I	Negative	Chip select signal
6	7	GND	I		Ground
7	—	GND	I		Ground
8	8	$\overline{\text{RD}}$	I	Negative	Read signal
9	9	A0	I	Positive	Address bus signal 0
10	10	$\overline{\text{WR}}$	I	Negative	Write signal
11	11	$\overline{\text{SYN0}}/\overline{\text{CLR}}$	O	N/N*1	Synchro. signal/servo deviation counter clear signal
12	12	D0	I/O	Positive	Data bus signal 0
13	13	D1	I/O	Positive	Data bus signal 1
14	14	D2	I/O	Positive	Data bus signal 2
15	15	D3	I/O	Positive	Data bus signal 3
16	16	D4	I/O	Positive	Data bus signal 4
17	—	VDD	I		+5V ±5%
18	17	D5	I/O	Positive	Data bus signal 5
19	18	D6	I/O	Positive	Data bus signal 6
20	19	D7	I/O	Positive	Data bus signal 7
21	20	GND	I		Ground
22	21	$\overline{\text{SD}-}$	I*2	Negative	Ramping-down signal (−) from mechanical system
23	22	$\overline{\text{SD}+}$	I*2	Negative	Ramping-down signal (+) from mechanical system
24	23	$\overline{\text{EL}-}$	I*2	Negative	End limit signal (−) from mechanical system
25	24	$\overline{\text{EL}+}$	I*2	Negative	End limit signal (+) from mechanical system
26	25	SUBCLK/ALM	I*2	P*1/P*1	Subclock/servo alarm (immeidate stop) signal
—	26	$\overline{\text{EC-Z}}$	I*2	Negative*1	Encoder Z-phase signal
27	27	$\overline{\text{POUT}}$	O	Negative*1	Common output pulse or plus direction output pulse
28	—	GND	I		Ground
29	28	PDIR	O	High*1	Direction signal or minus direction output pulse
30	29	HOLD	O	Positive	Pulse output status indication signal
31	30	FDOWN	O	Positive	Ramping-down indication signal
32	31	FKEEP	O	Positive	Constant-speed or cessation indication signal

Pin No.		Name	I/O	Logic	Description
MS	AS				
33	32	FUP	O	Positive	Ramping-up indication signal
34	33	LT	O	Positive	Preset counter status (R0 ≦ 0) indication signal
35	34	ZERO	O	Positive	Preset counter status (R0 = 0) indication signal
36	35	$\overline{\text{INT}}$	O*3	Negative	Interrupt request signal
—	36	$\overline{\text{EXTP}}$/$\overline{\text{EC-A}}$	I*2	N/N*1	Ext. pulse signal/encoder A-phase or up signal
—	37	INS/$\overline{\text{EC-B}}$	I*2	P/N*1	General-purpose signal/encoder B-phase or down signal
37	—	$\overline{\text{EXTP}}$	I*2	Negative	General-purpose input signal
38	—	INS	I*2	Positive	External pulse signal
39	—	VDD	I		+5V ±5%
40	38	$\overline{\text{ORG}}$	I*2	Negative*1	Origin return signal from mechanical system
41	39	$\overline{\text{SYN1}}$/$\overline{\text{INP}}$	I*2	N/N*1	Sync. signal/servo in-position signal
42	—	$\overline{\text{EC-A}}$	I*2	Negative*1	Encorder A-phase or up signal
43	—	$\overline{\text{EC-B}}$	I*2	Negative*1	Encoder B-phase or down signal
44	—	$\overline{\text{EC-Z}}$	I*2	Negative*1	Encoder Z-phase signal
—	40	VDD	I		+5V ±5%

Notes: *1. Default logic, which can be changed as desired.
*2. Input with pull-up resistor
*3. Open drain output (WIRED OR available)
PDIR signal is high level under the default condition.

6.2 Terminal Pin Functions (Pin No. in brackets)

6.2.1 VDD [MS: 17, 39] [AS: 40]
GND [MS: 6, 7, 21, 28] [AS: 3, 7, 20]

These are power input pins. Be sure to supply +5V ±5% to all VDD pins and connect all GND pins to the ground.

6.2.2 $\overline{\text{RESET}}$ Input [MS: 3] [AS: 4]

For normal operation of the internal circuit, you need to turn the $\overline{\text{RESET}}$ signal on once after turning the power on and input two clock signals during the time the $\overline{\text{RESET}}$ is turned on. For the reset conditions, refer to "4.5 Default (Reset) Conditions." If this signal is turned on during pulse output in progress, the LSI immediately stops generating pulses. Note that the last pulsewidth is not secured in such a case.

6.2.3 CLOCK Input [MS: 2] [AS: 2]

This pin inputs the reference clock. Usually, input the reference clock of 4.9152MHz or 9.8304MHz. Ouput pulses are produced referring to the clock input to this pin. Accordingly, the accuracy of output pulses depends on the reference clock. The clock is also used for internal control.

6.2.4 $\overline{\text{CS}}$ Input [MS: 5] [AS: 6]

This pin inputs the chip select signal. Putting the chip select signal at low level makes the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals valid, thereby allowing you to read or write data through the CPU.

6.2.5 $\overline{\text{RD}}$ Input [MS: 8] [AS: 8]

This pin inputs the read signal. Place both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins in low level. The status or register data will be output onto D0 to D7 of the data bus.

6.2.6 $\overline{\text{WR}}$ Input [MS: 10] [AS: 10]

This pin inputs the write signal. Change the signal level from low to high with the $\overline{\text{CS}}$ at low level. Data on data of D0 to D7 of the data bus will be written into the LSI.

6.2.7 A0 Input [MS: 9] [AS: 9] and A1 Input [MS: 4] [AS: 5]

These pins input address signals. Usually, they input low-place 2 bits of the address bus.

6.2.8 D0 to D7 [MS: 12, 13, 14, 15, 16, 18, 19, 20] [AS: 12, 13, 14, 15, 16, 17, 18, 19]

These pins form the bidirectional data bus. D0 is the least significant bit.

6.2.9 $\overline{\text{POUT}}$ Output [MS: 27] [AS: 27]
PDIR [MS: 29] [AS: 28]

These pins output motor control pulses. Under the default condition, the $\overline{\text{POUT}}$ pin outputs pulses and the PDIR pin outputs the direction signal. By setting bit 1 of the output mode command at 1, you can let the $\overline{\text{POUR}}$ pin output plus direction pulses and the PDIR pin output minus direction pulses. You can change the output logic by setting bit 11 of the R12 register. You can also mask the output for timer mode operation.

6.2.10 FDOWN Output [MS: 31] [AS: 30]

This pin outputs the FDOWN signal which allows you to monitor the operating status. The pin is placed in high level during ramping-down in progress.

6.2.11 FKEEP Output [MS: 32] [AS: 31]

This pin outputs the FKEEP signal which allows you to monitor the operating status. The pin is placed in high level during pulse output at a constant rate or in cessation.

6.2.12 FUP Output [MS: 33] [AS: 32]

This pin outputs the FUP signal which allows you to monitor the operating status. The pin is placed in high level during ramping-up (acceleration).

6.2.13 LT Output [MS: 34] [AS: 33]

This pin output the LT signal which allows you to monitor the operating status. The pin is placed in high level when the preset counter R0 counts down to a value equal or smaller than the ramping-down point set by the R6 register.

6.2.14 ZERO Output [MS: 35] [AS: 34]

This pin outputs the ZERO signal which allows you to monitor the operating status. The pin is placed in high level when the preset counter R0 counts down to 0.

6.2.15 HOLD Output [MS: 30] [AS: 29]

This pin outputs the HOLD signal which allows you to monitor the operating status. The pin is placed in high level during pulse output in cessation.

6.2.16 $\overline{\text{INT}}$ Output [MS: 36] [AS: 35]

This pin outputs the interrupt request signal to the CPU. Since it is an open drain output (with pull-up resistor), the pin is connected in WIRED OR. The pin is placed in low level during pulse output in cessation or at the start of deceleration in varied-speed preset mode operation.

If you place the LSI in the interchangeable mode with the 240K version by setting bit 3 of the output mode command at 0, the interrupt request at the start of deceleration is not available. The pin requires an external pull-up resitor of 5kΩ to 10kΩ.

6.2.17 OTS Output [MS: 1] [AS: 1]

This is a general-purpose output pin. You can control it with the register select command.

6.2.18 $\overline{\text{EL+}}$ [MS: 25] [AS: 24] and $\overline{\text{EL–}}$ [MS: 24] [AS: 23]

These pins input end limit signals from the mechanical system. When the end limit signal in the moving direction is turned on (placed in low level), the LSI immediately stops generating pulses and keeps the stop condition if the end limit signal is turned off thereafter. If the start mode command is written with the end limit signal turned on, the LSI does not generate any pulse. Notice that in such a case the LSI does not output any $\overline{\text{INT}}$ signal too.

You can check the ON/OFF status of end limit signal. Also, if output pulses are masked by setting bit 10 of the control mode register at 1, the $\overline{\text{EL}}$ signal does not stop the LSI from generating pulses. In this case too, you can check the input/output status of $\overline{\text{EL}}$ signal.

6.2.19 $\overline{\text{SD+}}$ Input [MS: 23] [AS: 22] and $\overline{\text{SD–}}$ Input [MS: 22] [AS: 21]

These pins input ramping-down signals from the external system. When the ramping-down signal in the moving direction is turned on (placed in low level), the LSI ramps down the pulse output. When the signal is turned off, the LSI ramps up the pulse output.

You can check the ON/OFF status of $\overline{\text{SD}}$ signal by reading the extension status register.

If the $\overline{\text{SD}}$ signals are made invalid with the control mode command, any $\overline{\text{SD}}$ signal does not start the LSI ramping down the pulse output. In this case too, you can check the ON/OFF status of the signal.

6.2.20 $\overline{\text{ORG}}$ Input [MS: 40] [AS: 38]

This pin inputs the origin return signal from the mechanical system. With bit 0 of the control mode command set at 1, the $\overline{\text{ORG}}$ signal which is turned on (placed in low level) immediately stops the LSI from generating pulses and keep the stop condition even if the $\overline{\text{ORG}}$ signal is turned off.

You can check the ON/OFF status of $\overline{\text{ORG}}$ signal even if the signal is made invalid by setting the control mode command.

6.2.21 $\overline{\text{EXTP}}$ Input [MS: 37] [AS: —]

This pin is provided for the PCL240MS only. Use this pin when you want to let the present counter R0 count down external signals.

6.2.22 INS Input [MS: 38] [AS: —]

This pin is provided for the PCL240MS only. The pin inputs a general-purpose signal. You can check the ON/OFF status by reading the status buffer.

6.2.23 $\overline{\text{EC-A}}$ Input [MS: 42] [AS: —]

This pin is provided for the PCL240MS only. Use the pin when you want to let the present position counter R10 count external signals.

6.2.24 $\overline{\text{EC-B}}$ Input [MS: 43] [AS: —]

This pin is provided for the PCL240MS only. Use the pin when you want to let the present position counter R10 count external signals.

6.2.25 $\overline{\text{EXTP}}$/$\overline{\text{EC-A}}$ Input [MS: —] [AS: 36)

This pin is provided for the PCL240AS only. For the $\overline{\text{EXTP}}$ signal input, set bit 2 of the output mode command at 1. For the $\overline{\text{EC-A}}$ signal input, set bit 7 of the R12 register at 1.

Input $\overline{\text{EXTP}}$ signals to this pin when you want to let the preset counter R0 count down external signals. Input $\overline{\text{EC-A}}$ signals to this pin when you want to let the present position counter R10 count external signals.

6.2.26 INS/$\overline{\text{EC-B}}$ Input [MS: —] [AS: 37]

This pin is provided for the PCL240AS only. If the pin is defined as the INS pin, it can be used for general purpose. You can check the ON/OFF status of the signal. Set bit 7 of the R12 register. The pin will be defined as the $\overline{\text{EC-B}}$ signal input. Use the pin as the $\overline{\text{EC-B}}$ input when you want to let the present position counter R10 count external signals.

6.2.27 $\overline{\text{EC-Z}}$ Input [MS: 44] [AS: 26]

You can include the number of encoder Z-phase signals in the conditions to complete an origin return. Use of the $\overline{\text{EC-Z}}$ signal increases the accuracy of origin return.

Though under the default condition each Z-phase signal is counted at the falling edge, you can change the logic by setting bit 12 of the R12 register. You can check the input status by reading bit 20 of the extension status register R17. Since with the PCL240AS the GND pin of the PCL-240AK was changed to the EC-Z pin, you may connect the pin to the ground if you do not use the function.

6.2.28 SUBCLK/ALM Input [MS: 26] [AS: 25]

This pin inputs the SUBCLK or ALM signal. Select either by setting bit 22 of the R12 register. The SUBCLK signal is the clock signal for special control. Refer to description on bits 8 to 10 of the R13 register. The ALM signal is the alarm signal from the motor driver. The ALM signal which is turned on immediately stops the LSI from generating pulses. The input logic can be changed by setting bit 13 of the R13 register and the ON/OFF status can be checked by reading bit 15 of the extension status register R17.

6.2.29 $\overline{\text{SYN1}}/\overline{\text{INP}}$ Input [MS: 41] [AS: 39]

This pin inputs either $\overline{\text{SYN1}}$ signal or $\overline{\text{INP}}$ signal. Set bit 0 of the output mode command at 1 to define the pin as the $\overline{\text{SYN1}}$ input. Set bit 9 of the R12 register at 1 to define the pin as the $\overline{\text{INP}}$ input.

If defined as the $\overline{\text{SYN1}}$ signal pin for synchronized operation of multiple units of LSI, input the $\overline{\text{SYN0}}$ signal to this pin for the main axis.

If defined as the $\overline{\text{INP}}$ signal pin, input the in-position signal from the servomotor to this pin. You can delay the output of $\overline{\text{INT}}$ signal until the $\overline{\text{INP}}$ signal is input. Also, if you use the pin as the $\overline{\text{INP}}$ pin, you can change the input logic.

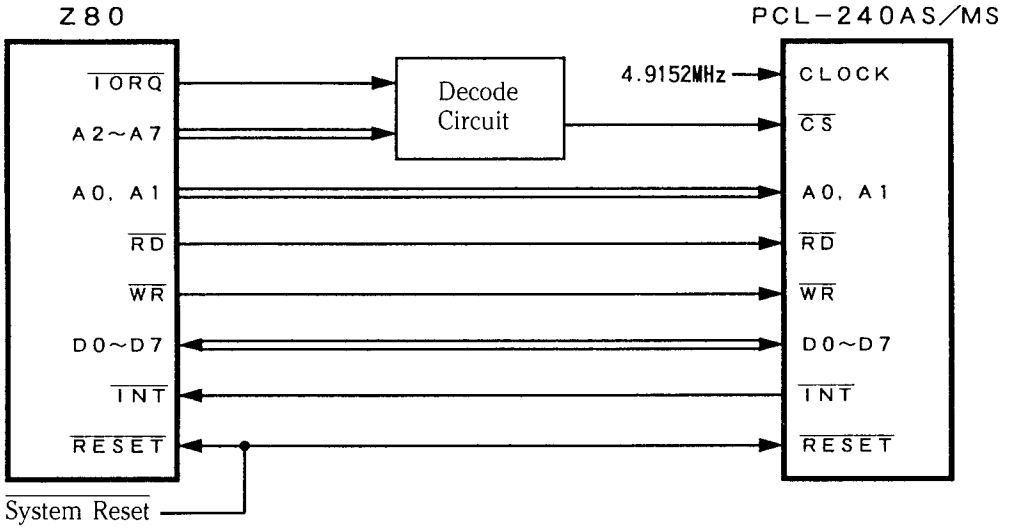
6.2.30 $\overline{\text{SYN0}}/\overline{\text{CLR}}$ Output [MS: 11] [AS: 11]

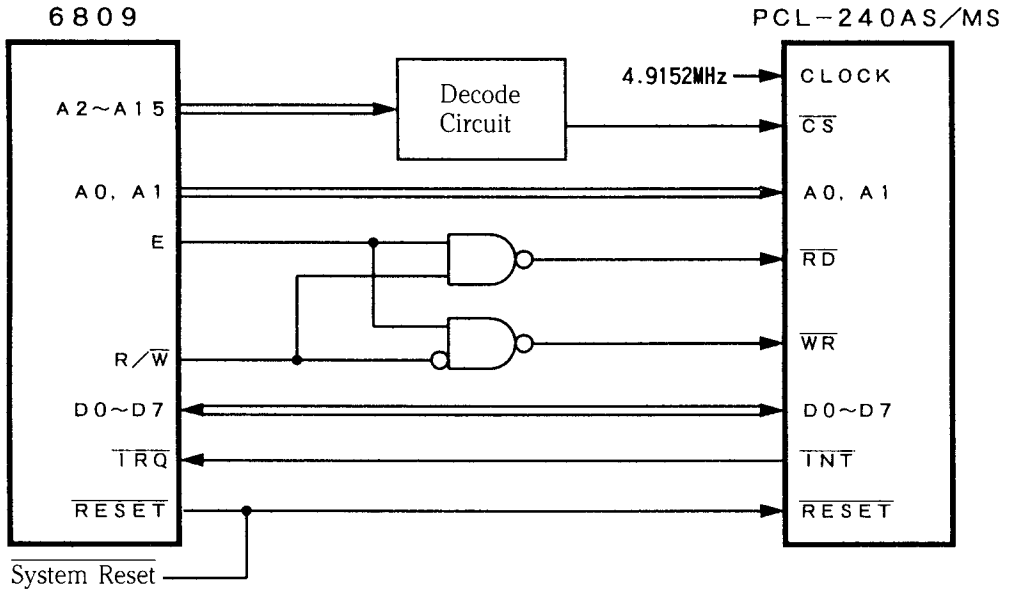
This pin outputs either $\overline{\text{SYN0}}$ or $\overline{\text{CLR}}$ signal, which is selected by bit 4 of the R13 register.

If defined as the $\overline{\text{SYN0}}$ pin, it outputs pulse signals for synchronized operation with multiple units of LSI.

The $\overline{\text{CLR}}$ signal is used to clear the deviation counter for immediate stop of the servomtor. The $\overline{\text{CLR}}$ signal with a time length of eight cycles of the reference clock is output when the $\overline{\text{EL}}$ signal stops the LSI from generating pulses or when an origin return is complete. You can change the output logic as well as outputting the signal with the command from the CPU.

6.3 Block Diagrams of CPU Interface Circuit





6.4 Precautions in Designing Hardware

- When the $\overline{\text{RESET}}$ signal is input, the $\overline{\text{RESET}}$ pin should be low level (ON) during a time length of more than two cycles of the reference clock.
- For safety, the LSI does not allow you to change the input logic of EL signals. If you need to change the logic, configure the external circuit for that purpose.
- Internal pull-up resistors (25kΩ to 500kΩ) of $\overline{\text{EL}}$ and other pins (refer to "6.1 Terminal Pin Assignment") are provided to prevent floating. Connect external pull-up resistors as required.
- The $\overline{\text{INT}}$ pin has a built-in pull-up resistor. But since the resistance is high, the pin requires an external pull-up resistor of 5kΩ to 10kΩ.

7. Characteristics

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
Input Current	I_{IN}	±10	mA
Storage Temperature	T_{stg}	−40 to +125	°C

7.2 Recommended Operating Conditions

Item	Symbol	Rating	Unit
Power Voltage	V_{DD}	4.75 to 5.25	V
Ambient Temperature	T_J	0 to +70	°C

7.3 DC Characteristics

Item	Symbol	Condition	Min.	Max.	Unit
Static Current Consumption 1	I_{DD1}	Note 1		30	μA
Static Current Consumption 2	I_{DD2}	Note 2		3.2	mA
Current Consumption	I_{DD3}	Note 3		10	mA
Output Leakage Current	I_{OZ}	Note 4	−10	10	μA
		Note 5	−200	10	μA
Low Level Input Current	I_{IL}	Note 6	−10	10	μA
		Note 7	−200	−10	μA
High Level Input Current	I_{IH}		−10	10	μA
Low Level Input Voltage	V_{IL}			0.8	V
High Level Input Voltage	V_{IH}		2.2		V
Low Level Output Current	I_{OL}	Notes 4 & 5		8	mA
High Level Output Current	I_{OH}	Note 4		−8	mA
Low Level Output Voltage	V_{OL}	I_{OL} = 1μA		0.05	V
		I_{OL} = 8mA		0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = −1μA	V_{DD} − 0.05		V
		I_{OH} = −8mA	2.4		V
Internal Pull-up Resistance	R_{UP}		25	500	kΩ

NOTES: 1. CLK = 0Hz, input with pull-up resistor = V_{DD} level, $\overline{INT}$ signal = OFF
2. CLK = 0Hz, input with pull-up resistor = 0V, $\overline{INT}$ signal = ON
3. CLK = 4.9152MHz, output frequency = 2.4573MHz, no load
4. D0-D7, OTS, $\overline{SYN0}/\overline{CLR}$, $\overline{POUT}$, PDIR, HOLD, FDOWN, FKEEP, FUP, LT, ZERO
5. $\overline{INT}$
6. $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, D0-D7, CLK, $\overline{RESET}$
7. $\overline{EC\text{-}A}$, $\overline{EC\text{-}B}$, $\overline{EC\text{-}Z}$, INS, $\overline{EXTP}$, $\overline{EXTP}/\overline{EC\text{-}A}$, INS/$\overline{EC\text{-}B}$, SUBCLK/ALM, $\overline{SYN1}/\overline{INP}$, $\overline{EL+}$, $\overline{EL-}$, $\overline{SD+}$, $\overline{SD-}$, $\overline{ORG}$

7.4 AC Characteristics

7.4.1 Reference Clock

Item	Symbol	Condition	Min.	Max.	Unit
Reference Clock Frequency	f_{CLK}			10	MHz
Cycle of Reference Clock	T_{CLK}		100		ns
Time Width of High Level	T_{CKH}		40		ns
Time Width of Low Level	T_{CKL}		40		ns

7.4.2 Read Cycle

Item	Symbol	Condition	Min.	Max.	Unit
Address Stabilizing Time	t_{AR}		0		ns
Address Holding Time	t_{RA}		0		ns
Read Pulsewidth	t_{RR}		24		ns
Data Delay Time	t_{RD}	C_L=40pF		24	ns
Data Floating Delay Time	t_{DF}	C_L=40pF		21	ns

7.4.3 Write Cycle

Item	Symbol	Condition	Min.	Max.	Unit
Address Stabilizing Time	t_{AW}		0		ns
Address Holding Time	t_{WA}		0		ns
Write Pulsewidth	t_{WW}		33		ns
Data Setup Time	t_{DW}		23		ns
Data Holding Time	t_{WD}		0		ns

7.4.4 Reset Cycle

Item	Symbol	Condition	Min.	Max.	Unit
RESET Pulsewidth	t_{RST}		3		t_{CLK}
Resetting Time	t_{RSTM}			1	t_{CLK}

Note: The unit "t_{CLK}" is a time length of one cycle of reference clock.

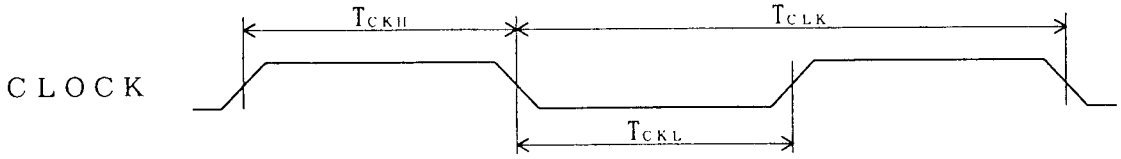
7.4.5 Operation Timing

Item	Symbol	Condition	Min.	Max.	Unit
$\overline{POUT}$ Delay Time H→L	t_{PLD}	C_L=40pF		23	ns
$\overline{POUT}$ Delay Time L→H	t_{PHD}	C_L=40pF		19	ns
FUP Delay Time L→H	t_{FUPH}	C_L=40pF		18	ns
FUP Delay Time H→L	t_{FUPL}	C_L=40pF		18	ns
FKEEP Delay Time L→H	t_{FKPH}	C_L=40pF		18	ns
FKEEP Delay Time H→L	t_{FKPL}	C_L=40pF		18	ns
FDOWN Delay Time L→H	t_{FDWH}	C_L=40pF		18	ns
FDOWN Delay Time H→L	t_{FDWL}	C_L=40pF		18	ns
$\overline{EL}$ Pulsewidth $\overline{ORG}$, ALM)	t_{EL}	High sensi.	18		ns
$\overline{EL}$ → $\overline{INT}$ Delay Time	t_{ELI}	C_L=40pF		33	ns
Preset → $\overline{INT}$ Delay Time	t_{PI}	C_L=40pF		35	ns
$\overline{EL}$→HOLD Delay Time L→H	t_{EHDH}	C_L=40pF		25	ns
Preset→HOLD Delay Time L→H	t_{PHDH}	C_L=40pF		27	ns
HOLD Delay Time H→L	t_{HDL}	C_L=40pF		22	ns
$\overline{CLR}$ Delay Time	t_{CLR}	C_L=40pF		26	ns
LT Delay Time L→H	t_{LTH}	C_L=40pF		18	ns
ZERO Delay Time L→H	t_{ZRH}	C_L=40pF		17	ns
$\overline{EC}$-$\overline{A}$/$\overline{B}$ High Level Time 1	t_{ECH1}		3		t_{CLK}
$\overline{EC}$-A/$\overline{B}$ High Level Time 2	t_{ECH2}		1.5		t_{CLK}
$\overline{EC}$-$\overline{A}$/$\overline{B}$ Low Level Time 1	t_{ECL1}		3		t_{CLK}
$\overline{EC}$-$\overline{A}$/$\overline{B}$ Low Level Time 2	t_{ECL2}		1.5		t_{CLK}
$\overline{EC}$-A/$\overline{B}$ Phase Diff. Time	t_{EAB}		1.5		t_{CLK}
Register Data Read Interval	t_{DRD}		2		t_{CLK}
Register Data Write Interval	t_{DWR}		2		t_{CLK}

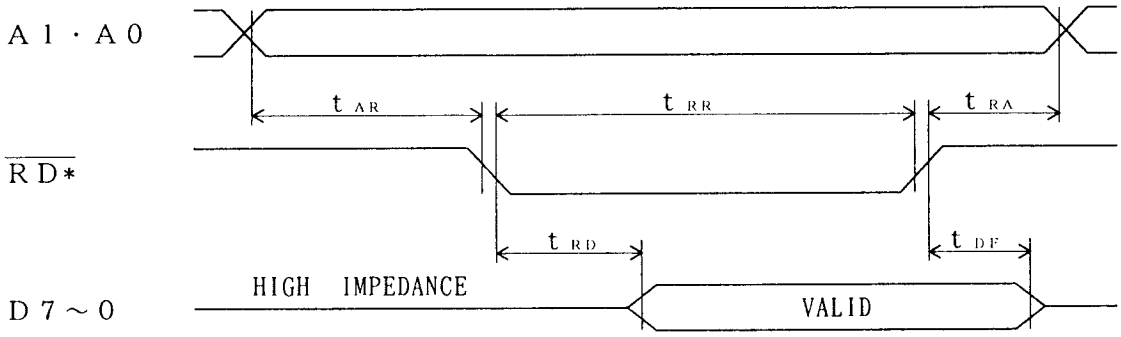
Note: The unit "t_{CLK}" is a time length of one cycle of reference clock.

7.5 Timing Charts

7.5.1 Reference Clock

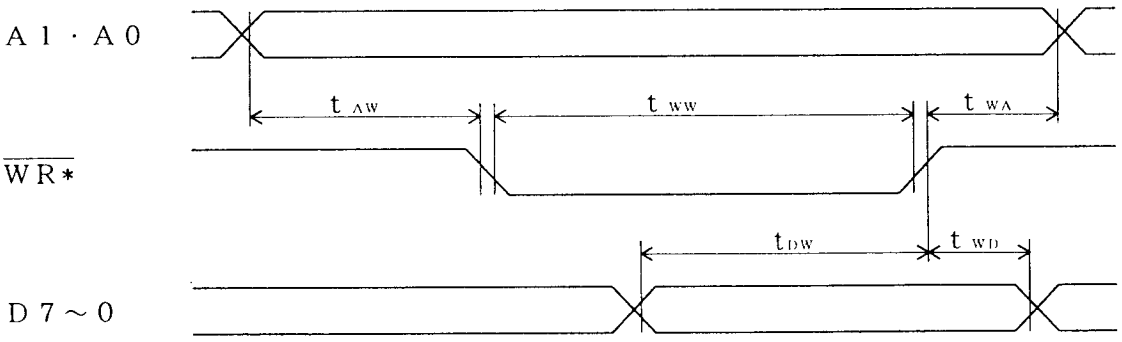


7.5.2 Read Cycle



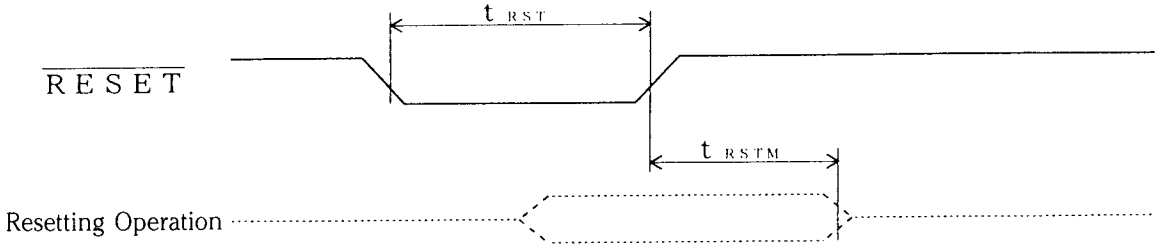
$\overline{RD*} = \overline{RD} \cdot \overline{CS}$ (logical product)

7.5.3 Write Cycle



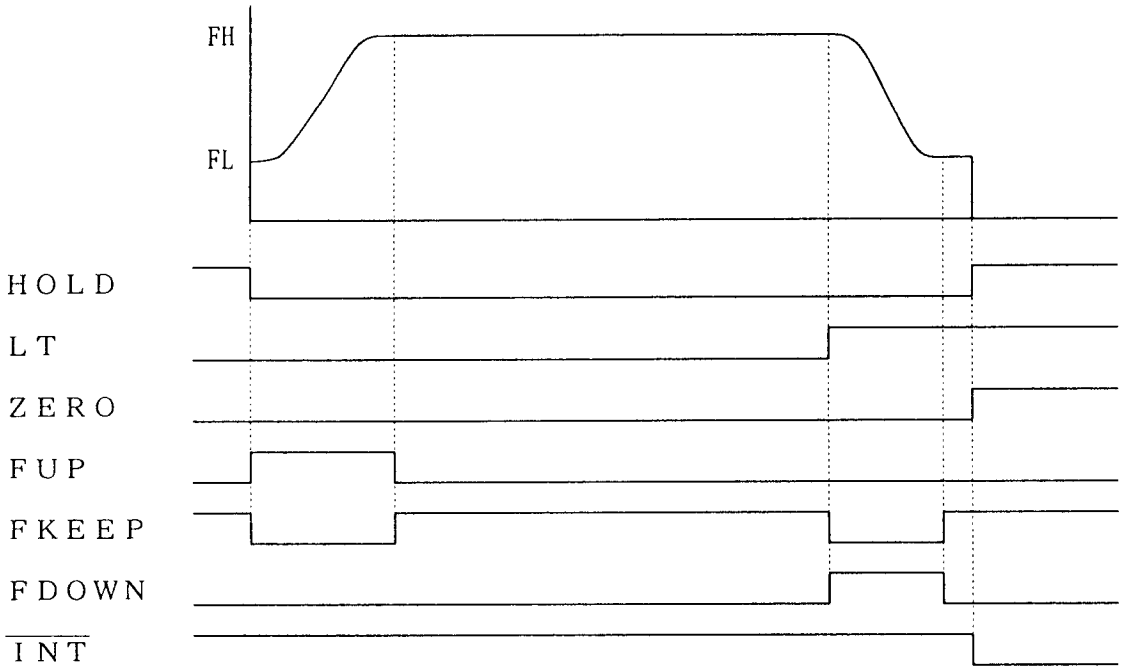
$\overline{WD*} = \overline{WD} \cdot \overline{CS}$ (logical product)

7.5.4 Reset Cycle

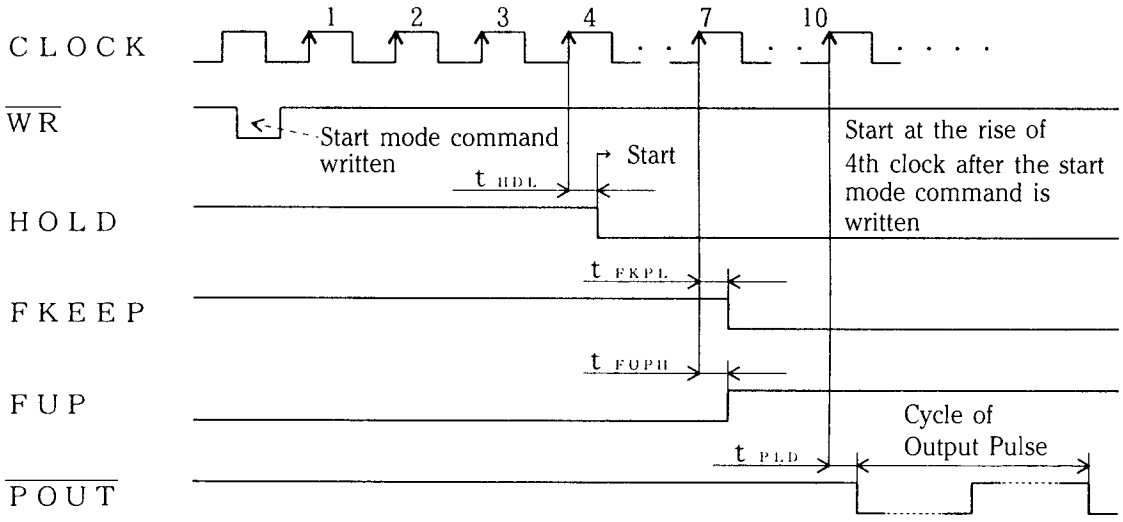


7.5.5 Timing of HOLD, LT, ZERO, FUP, FKEEP, FDOWN and $\overline{\text{INT}}$ Signals

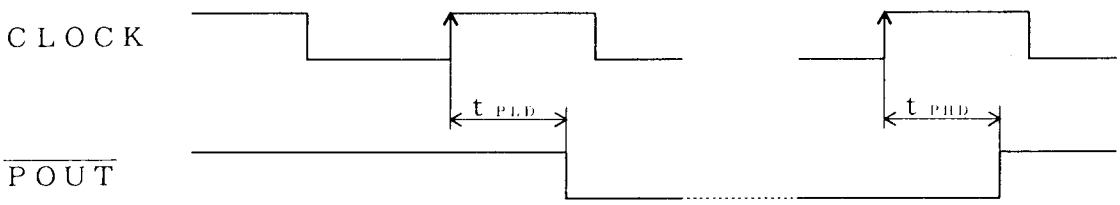
(Varied-speed operation in preset mode)



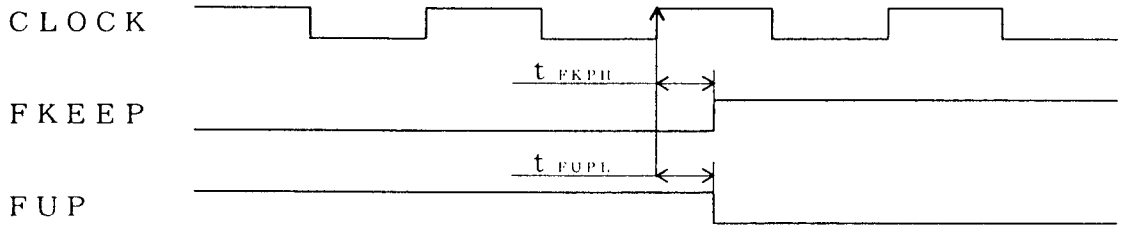
7.5.6 Start Timing (with $\overline{\text{POUT}}$ = Negative Logic)



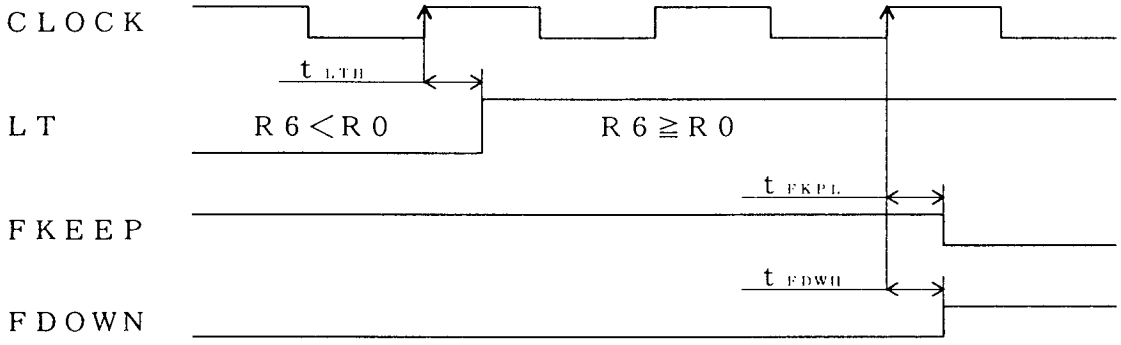
7.5.7 $\overline{\text{POUT}}$ Timing ($\overline{\text{POUT}}$ = Negative Logic)



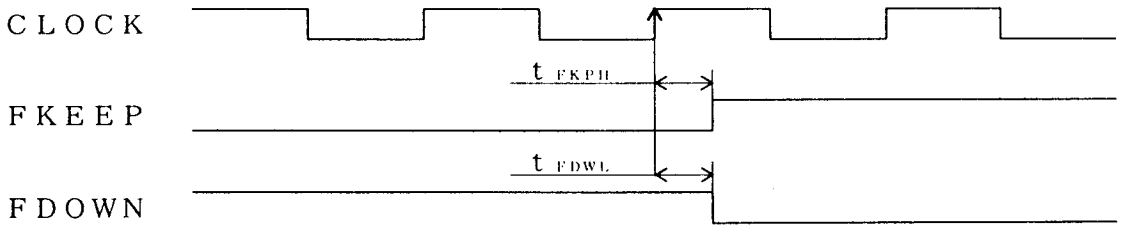
7.5.8 Ramping-up Completion Timing



7.5.9 Ramping-down Start Timing

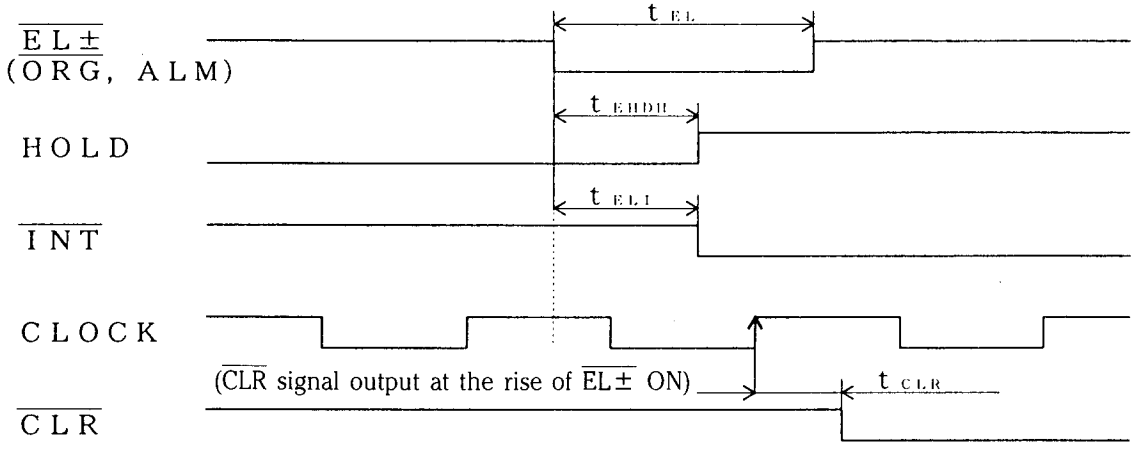


7.5.10 Ramping-down Completion Timing

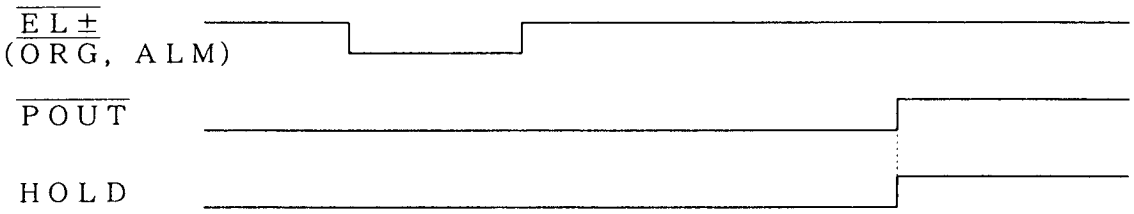


7.5.11 Timings at the Stop of Pulse Output (POUT = Negative Logic)

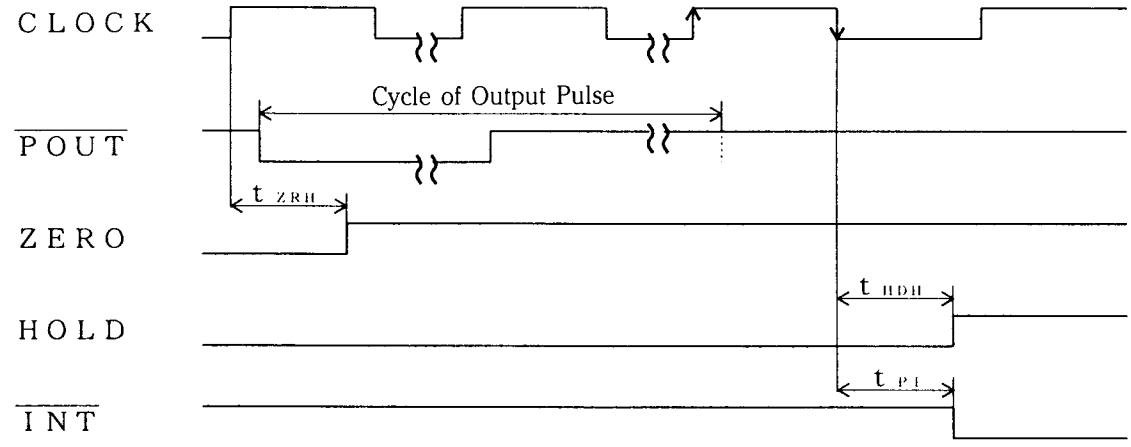
● Stop due to $\overline{EL\pm}$, $\overline{ORG}$ or ALM Signal



If the $\overline{EL}$ signal is turned on during pulse output in progress, the $\overline{POUT}$ stops outputting pulses upon completing the cycle of the last pulse.



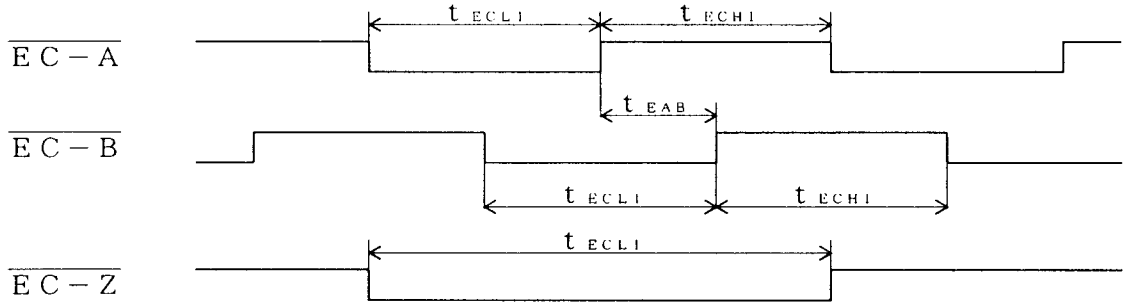
● Stop due to Completion of Preset Mode Operation



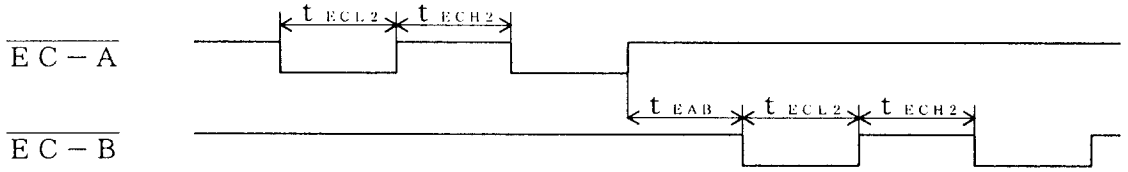
7.5.12 $\overline{\text{EC-A}}/\overline{\text{EC-B}}$ Timing

In the case of inputting 90° phase difference signals, a maximum acceptable response frequency is one-sixth of the reference clock. In the case of inputting plus and minus pulses, a maximum acceptable response frequency is one-third of the reference clock.

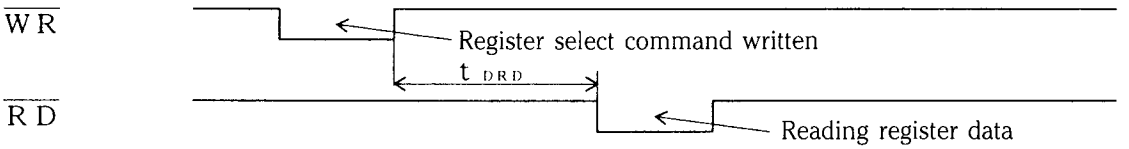
- In the case of inputting 90° phase difference signals



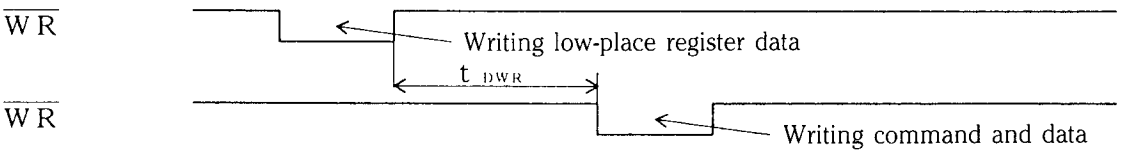
- In the case of inputting plus and minus pulses



7.5.13 Timing to Collectively Read Data from Register



7.5.14 Timing to Collective Write Data to Register



8. Handling Precautions

8.1 Designing Precautions

(1) In any case the LSI shall not be subjected to a condition exceeding the absolute maximum ratings.

(2) Protect the LSI from receiving a heating effect from environment and keep ambient temperatures as lowest possible.

(3) A latch-up condition may cause heat generation and fuming. Take the following precautions:

- Do not make the voltage level of input/output pins higher than V_{DD} and lower than GND. Also, take the power-up timing into consideration.
- Do not apply abnormal noise to the LSI.
- Fix the potential of unused input/output pins to V_{DD} or GND.
- Do not short-circuit the output.
- Protect the LSI against induction and static electricity from a high-voltage generation circuit.

(4) Take care that an excess voltage due to noise, surge and static electricity is not applied to the LSI.

8.2 Transportation and Storage Precautions

(1) Handle the package gently. Throwing or dropping it may damage the LSI in it.

(2) Do not store the package where it may be splashed with water or exposed to direct sunlight.

(3) Do not store the package where poisonous or corrosive gases are generated.

(4) Prepare an anti-static container and take care that the LSI may not receive any load.

8.3 Assembling Precautions

(1) Take the following precautions to protect the LSI against damage due to static electricity:

- Ground the instruments and fixtures which are installed at the assembling area.
- Ground the worktable with a conductive mat or the like having resistance. Avoid the metal surface which may cause an abrupt electrical discharge with low resistance if the electrified LSI contacts with the surface.
- When picking up the LSI with vacuum, mount a conductive rubber or the like onto the tip of pickup to prevent the LSI from being electrified. Also, use contacts featuring highest possible resistance for connection to lead terminals of LSI.

- Tweezers which may contact with pins of the LSI should be resistant against static electricity. Avoid metal tweezers if possible.
- Put the LSI mounted boards in the board holder which is protected against electrification. Do not put them one over another. If you do so, friction may cause electification and discharge.

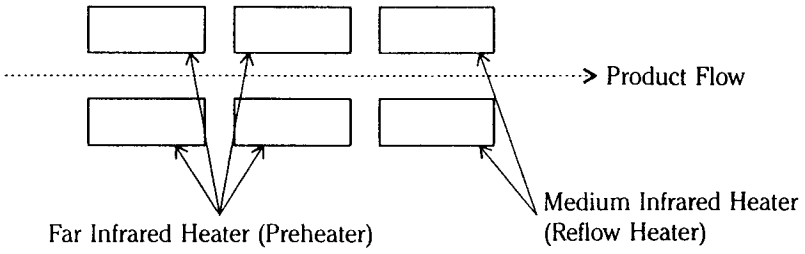
(2) The worker should wear a wrist strap, which should be grounded via 1MΩ resistor.

(3) Use a low-voltage soldering iron and ground it at the tip.

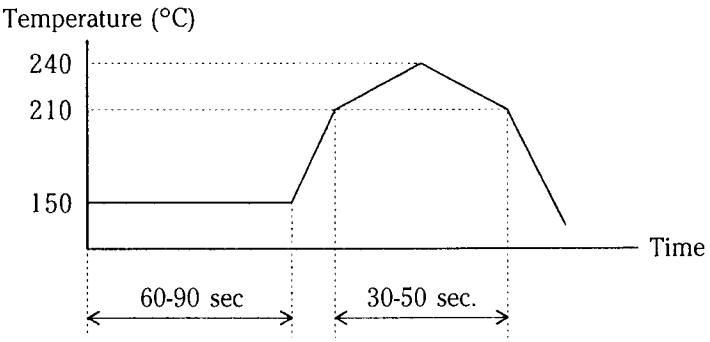
(4) Do not place the LSI or the container near the instruments, such as CRT, which generate a high electrical field.

(5) If the fully heating soldering method is used, conduct high-temperature dehumidifying treatment at 125°C for 20 hours.

(6) If soldering is made through an infrared reflow method for reduction of heat stress, the far and medium infrared reflow method is recommended.



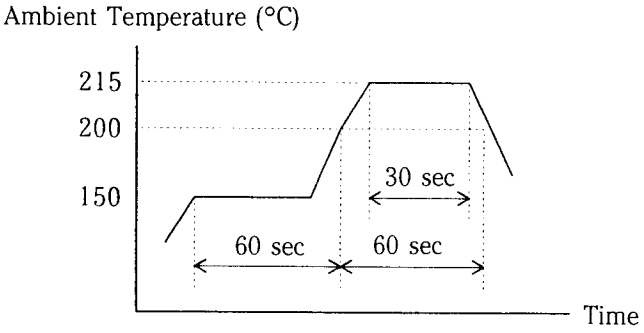
Soldering should be done in such a manner that the time length the package surface and PC board surface are heated to a range of 210°C to 240°C maximum in 30 to 50 seconds. At the time of reflow, cooling should be done at a rate of lower than 3°C per second.



(7) For the warm-air reflow, use the same procedure as the far infrared reflow method.

(8) For the vapor phase soldering, Florinade FC-704 or the equivalent is recommended as the solution. Time lengths of heating should be within 30 seconds at 215°C and within 60 seconds at 200°C.

(9) In the case of soldering iron, soldering should be done within 10 seconds at maximum 260°C at the lead or within 3 seconds at maximum 350°C at the lead.



8.4 Other Precautions

(1) If the LSI is intended for use under adverse environmental conditions (humidity, corrosive gases or dirt), take proper measures such as humidity-resistant coating.

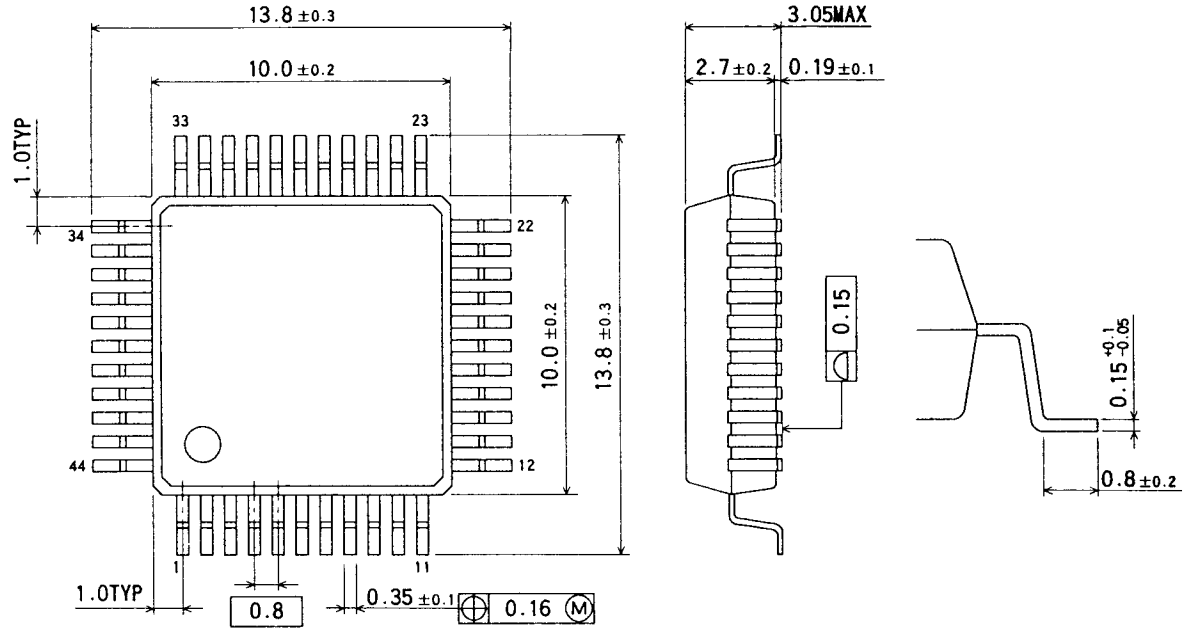
(2) Resin materials used for the package are flame-retardant but not non-inflammable. So it may be burned or fume. Avoid placing it near an inflammable material.

(3) The LSI is designed for office appliances, communications equipment, measuring instruments and home electric appliances. If you use it for the system of which a trouble or erroneous operation may lead to the death or injure the operator, such as nuclear control system, space ship, traffic signal, combustion control system or safety device, take sufficient care.

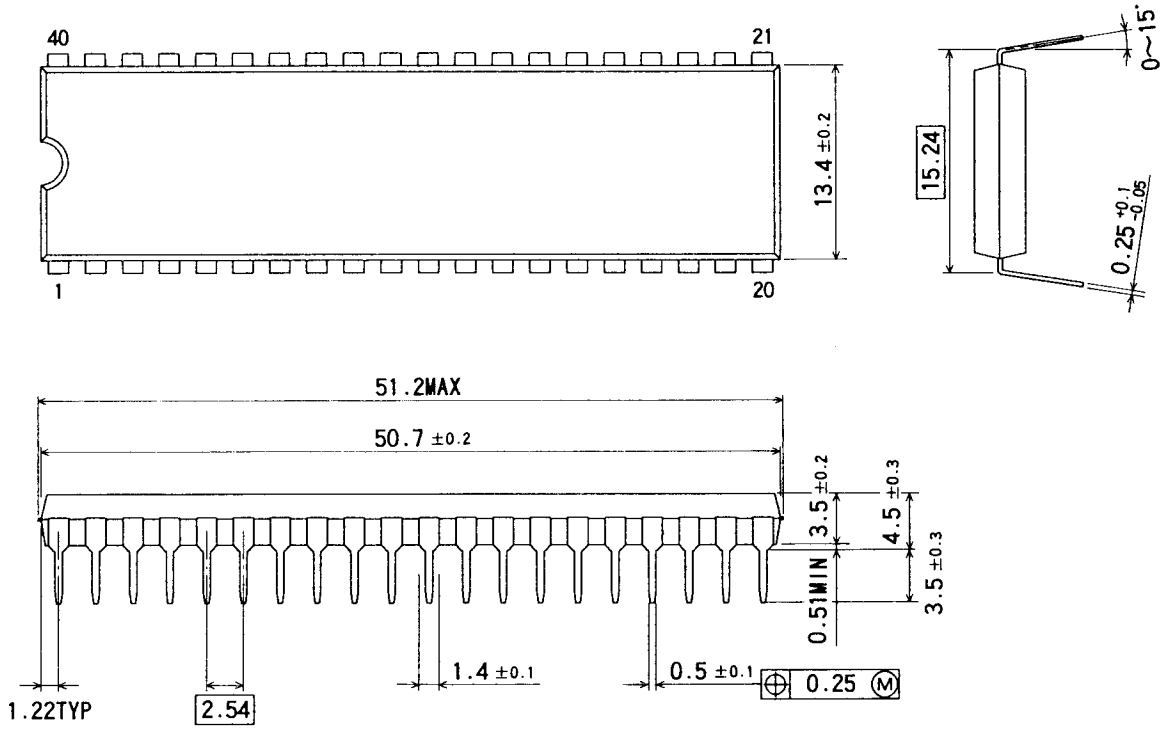
9. External Dimensions

9.1 PCL240MS

Unit: mm



9.2 PCL240AS



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