USER'S MANUAL

PROGRAMMABLE SINGLE-CHIP HIGH-SPEED PULSE GENERATORS

PCL5014

NPM NIPPON PULSE MOTOR CO., LTD.

CONTENTS

Considerations in Reading this User's Manual

(1) Varied-speed operation means pulse output in varied rates including S-curve or linear acceleration/deceleration.
(2) Constant-speed operation means pulse output at a constant rate with no acceleration/deceleration.
(3) The input/output logic of each pin indicates the logic under the reset condition.
(4) "Plus (+)" in the description indicates incremeting the up/down counter.
(5) "Minus (−)" in the description indicates decrementing the up/down counter.

1. General Description

The PCL5014 is a CMOS LSI. It oscillates high-frequency pulses to drive stepping motors and pulse train input servomotors according to commands transferred through the CPU bus interface. Thus, using this CMOS LSI, you can perform continuous motion control, in-positioning and origin return in various ways including constant speed, linear acceleration/deceleration and S-curve acceleration/deceleration.

Furthermore, you can control the output pulses and check the operation status of PCL5014 by sending signals from an external instrument as well as letting it oscillate pulses according to an interrupt signal based on conditions.

The PCL5014 is also provided with a function to control servomotor drivers, that accept pulse & direction command.

Our sophisticated design concept lets you easily access to the versatile functions with simple commands while reducing the burden to the CPU.

Features

- S-curve acceleration/deceleration control (acceleration/deceleration parameters can be independently set)
- Automatic adjustment of maximum speed for less movement amount
- Applicable to drivers with microstep control function
- Maximum output frequency of 4.9 Mpps with a reference clock of 19.6608MHz
- Parameters for the next operation can be written in preregisters while the present operation is in progress.
- Out-of-step detection for stepping motor
- Output of idling pulses
- Interface for servomotor control
- External pulse input
- Interface to Intel or Motorola CPU
- Connectable to 8-bit or 16-bit data bus
- 8- or 16-byte address area
- Origin return in 12 ways
- Setting of signed parameter available for moving amount
- Setting of moving amount available on the basis of absolute position
- Up/down counter
- Two built-in comparator circuits
- 3-bit universal I/O ports with interrupt function
- Simultaneous start function
- Simultaneous stop at an abnormal event

2. Specifications

2.1 Specifications

Power Requirement: +5V ±5%

Reference Clock: 19.6608MHz standard (25MHz maximum)

Positioning Pulse Rate Setting Range: 0 to 268,435,455

Pulse Rate Setting Steps: 1 to 32,767

Pulse Rate Multiplication Setting Range: 0.1 to 150 times
0.1 to 3,276.7 pps with 0.1x
1 to 32,767 pps with 1x
150 to 4,915,050 pps with 150x

Pulse Rate Setting Registers: Two types of FL and FH

Ramping-down Point Setting Range: 0 to 16,777,215

Acceleration/Deceleration Rate Setting Range: 1 to 65,535 (can be independely set for acceleration and deceleration)

Up/Down Counter Counting Range: 0 to 268,435,455, or
−134,217,728 to +134,217,727

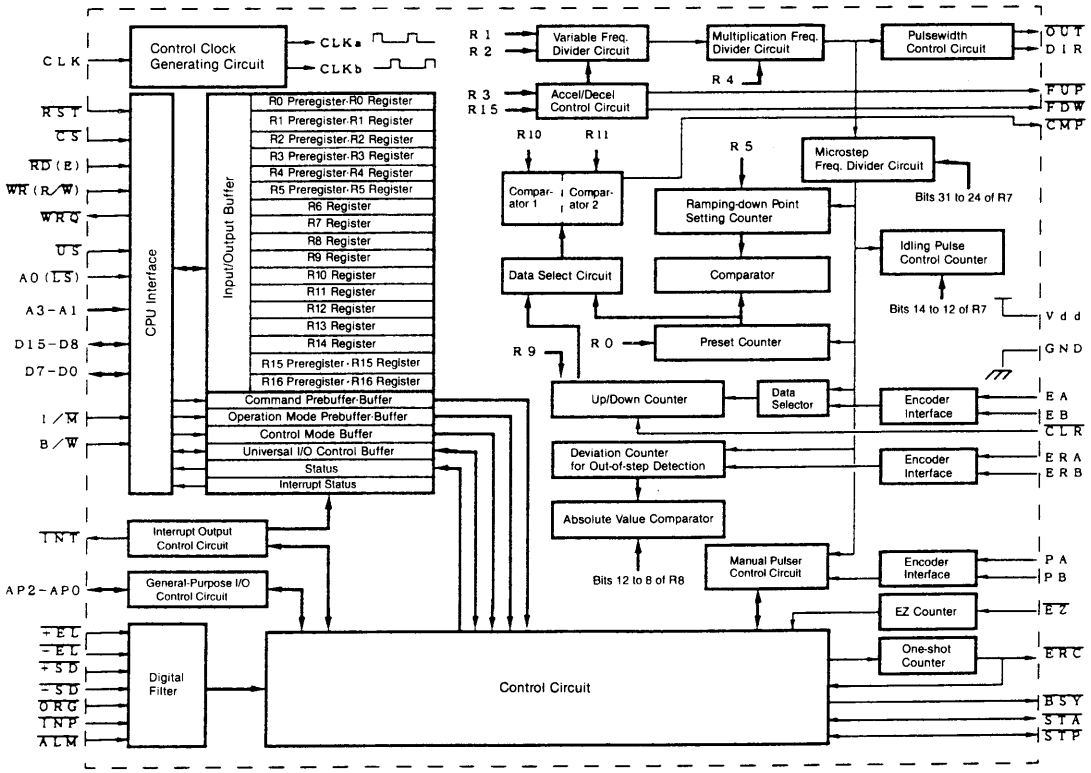
Major Operations Available:
- Continuous operation
- Preset operation
- Origin return
- Origin search
- Origin escape
- Zero return
- One-pulse output
- Timer mode operation

Operating Temperature Range: 0 to +70°C

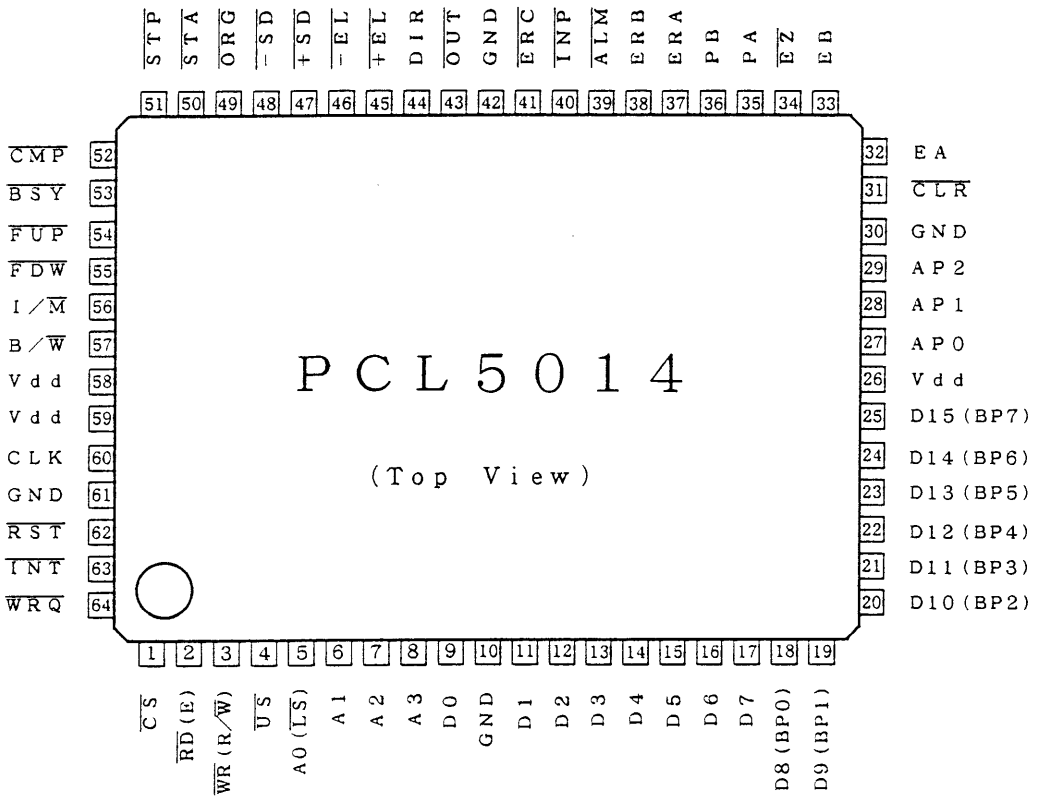
Storage Temperature Range: −40 to +125°C

Package: 64-pin QFP

2.2 Block Diagram



2.3 Terminal Pin Layout

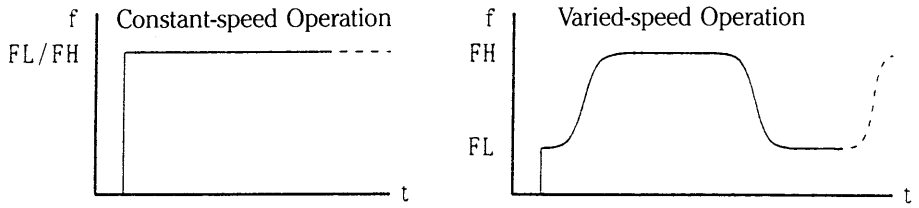


3. Outline of Functions

The PCL5014 starts and stops generating pulses according to commands from the CPU to control the stepping motor or servomotor. By writing desired parameters to the PCL5014, you can control the motor in various ways. This chapter describes terms and the outline of each function. For detailed operation, see the chapter 5.

3.1 Pulse Output Patterns

The PCL5014 allows you to select a pulse output pattern of either constant-speed operation or varied-speed operation.



3.1.1 Constant-speed Operation

The PCL5014 outputs pulses at a fixed frequency to control the motor at a constant speed from the start to end. As the fixed frequency, you can select either the FL pulse rate (low speed) or FH pulse rate (high speed).

3.1.2 Varied-speed Mode

The PCL5014 starts outputting pulses at the FL pulse rate, then increases the frequency to the FH pulse rate, which ramps down to the FL rate before termination. Thus, the motor is driven at a high speed with an acceleration at the start and a deceleration at the end.

The PCL5014 provides the S-curve mode for mild acceleration/deceleration and the linear mode for sharp acceleration/deceleration.

3.2 Commands

You can operate the PCL5014 by writing commands from the CPU to the designated address (command buffer). There are eight basic commands. The resultant operations depend on written data.

3.2.1 Start Command

The Start command starts the PCL5014 outputting pulses in the constant-speed or varied-speed mode as written in the command. If you write the start command during in-positioning in progress, it will be used to automatically start the next operation.

3.2.2 Pulse Rate Switchover Command

The pulse rate switchover command lets the PCL5014 switch the current pulse rate from the FL to FH or vice versa with or without acceleration/deceleration as written in the command.

3.2.3 Stop Command

The stop command stops the PCL5014 from outputting pulses either immediately or with a deceleration before stop.

3.2.4 Start Retention Command

The start retention command lets the PCL5014 suspend pulse output. Using this command and $\overline{\text{STA}}$ pin, you can simultaneously start multiple units of PCL5014.

This command written during in-positioning in progress will be used to automatically start the next operation.

3.2.5 General-Purpose I/O Bit Control Command

The general-purpose I/O bit control command places the AP and BP pins which are set for output, at low or high level.

3.2.6 Control Command

The control command sets or resets the internal controller. It allows you, for example, to reset the counter or stop the PCL5014 in an emergency.

3.2.7 Register Read Command

The register read command lets the CPU read numerical or control data from a designated register.

3.2.8 Register Write Command

The register write command lets the CPU write numerical or control data into a designated register.

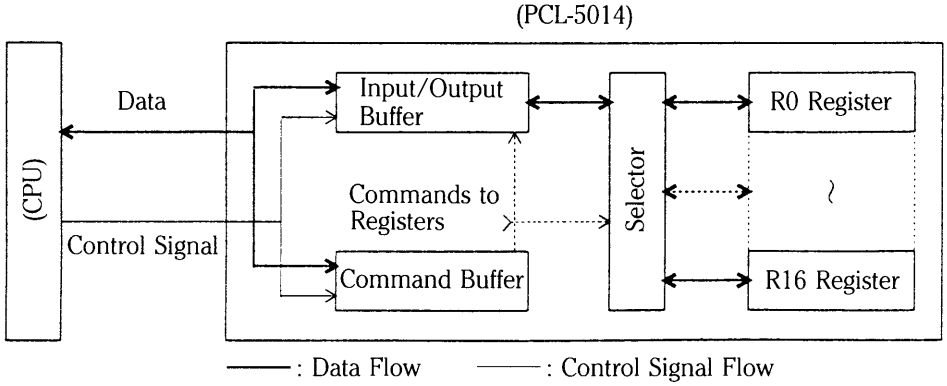
3.3 Registers

Registers store numerical data (pulse rates, number of output pulses, etc.) and control data (logics set for input/output pins, etc.). The register data are read or written to/from the CPU via the input/output buffer with the register read or register write command.

3.3.1 Input/Output Buffer

The input/output buffer put between the CPU interface and registers temporarily stores register data at the time of reading or writing data to/from the CPU. The register read command lets the input/output buffer read the data once and then the CPU read the data from the input/output buffer. The register write command lets the CPU write the data into the input/output buffer once and then the input/output buffer write the data into a register. The input/output buffer provides a bit length of 32 bits and reads or writes data by dividing it into 8 bits (or 16 bits) while selecting addresses.

3.3.2 Data Flow from/to Registers



3.3.3 Direct Ports

Register data and some internal counter values can be read directly from addresses of direct ports 1 and 2.

3.3.4 Register Functions

PCL5014 provides registers R0 to R16 and preregisters R0 to 5, R15 and R16. Preregisters allow you to set parameters for the next operation during present operation in progress.

R0 Resister/R0 Preregister, Preset Number of Output Pulses

The R0 register and R0 preregister are for the number of output pulses to move the motor in a target amount. Write the number of output pulses in the R0 preregister.

R1 Register/R1 Preregister, FL Pulse Rate

The R1 register and R1 preregister are for the FL pulse rate. In the varied-speed mode, the rate is used at the start of acceleration and at the end of deceleration.

Notice that a practical pulse output rate is a product of the rate entered here and a multiplication factor entered in the R4 register.

Write the FL pulse rate in the R1 preregister. Use the R1 register to change the rate during operation in progress.

R2 Register/R2 Preregister, FH Pulse Rate

The R2 register and R2 preregister are for the FH pulse rate. In the varied-speed mode, the rate is used in the meantime between acceleration and deceleration.

Notice that a practical pulse output rate is a product of the rate entered here and a multiplication factor entered in the R4 register.

Write the FH pulse rate in the R2 preregister. Use the R2 register to change the rate during operation in progress.

R3 Register/R3 Preregister, Acceleration Rate

The R3 register and R3 preregister are for the acceleration rate.
Write the acceleration rate in the R3 preregister. Use the R3 register to change the rate during operation in progress.

R4 Register/R4 Preregister, Multiplication Factor

The R4 register and R4 preregister are for the multiplication factor which multiplies the pulse rates entered in R1 and R2.

R5 Register/R5 Preregister, Ramping-down Point

The R5 register and R5 preregister are for the ramping-down point used in the varied-speed operation and in-positioning.
If the ramping-down point is set manually or if the number of pulses required for deceleration is set automatically, set R5 to zero or an offset value. Write the ramping-point in the R5 preregister.

R6 Register, Environment Setting 1

The R6 register sets logics of input/output pins, operations at signal input and other, 29 particulars in total.

R7 Register, Environment Setting 2

The R7 register sets origin return conditions, the number of output pulses, comparator control conditions, etc., 13 particulars in total.

R8 Register, Environment Setting 3

The R8 register sets interrupt signal generating conditions at the $\overline{\text{INT}}$ pin and other, 12 particulars in total.

R9 Register, Up/Down Counter

The PCL5014 is equipped with an up/down counter for position control. The R9 register allows you to write/read the up/down counter value.

R10 Register, Comparator 1 Data

The PCL5014 is equipped with two comparactor circuits for comparison of data with the up/down counter value.
The R10 register allows you to write/read the comparator 1 data.

R11 Register, Comparator 2 Data

The R11 register allows you to write/read the comparator 2 data.

R12 Register, Counter Monitor

The read-only register allows you to read four types of data including set pulse rates.

R13 Register, Command Monitor 1

This read-only register allows you to read applied commands, mode settings, etc.

R14 Register, Command Monitor 2

This read-only register allows you to read commands, the mode and other particulars which will be used for the next operation.

R15 Resister/R15 Preregister, Deceleration Rate

The R15 register and R15 preregister are for the deceleration rate. If "0" is entered here, the acceleration rate entered in R3 will be used as the deceleration rate.

Write the deceleration rate in the R15 preregister. Use the R15 register to change the rate during operation in progress.

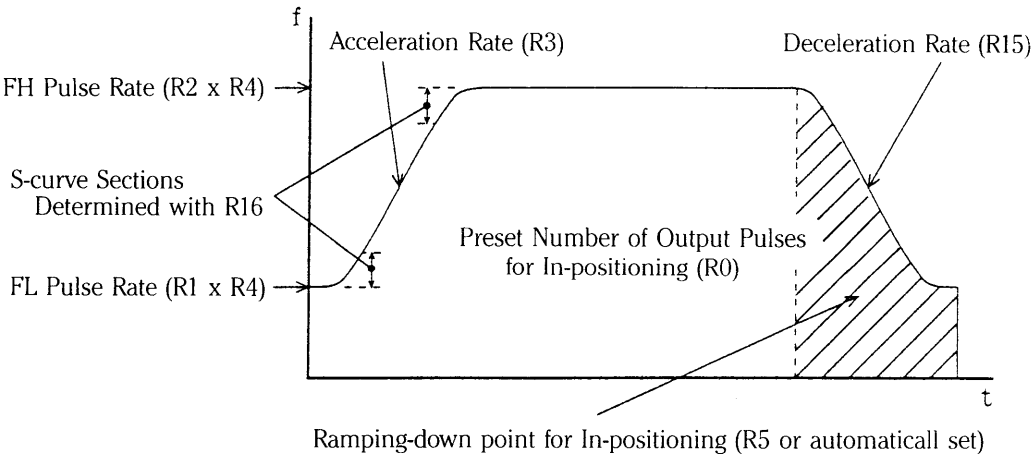
R16 Register/R16 Preregister, S-curve Section

If you want to put a linear acceleration/deceleration at the mid-point of S-curve acceleration/deceleration, write the parameter in the R16 preregister. Use the R16 register to change the parameter during operation in progress.

Other Reading Data

Besides register data, the register read command allows you to read the counting of output pulses for in-positioning and the counting of the ramping-down point used for the automatic deceleration in the varied-speed operation or in-positioning.

3.3.5 Register Data Applied Points on Pulse Output Pattern



3.4 Counters

The PCL5014 provides the preset counter for in-positioning and the ramping-down point counter for automatic deceleration in the varied-speed operation or in-positioning.

3.4.1 Preset Counter

The preset counter is used for in-positioning. When the PCL5014 starts outputting pulses, the preset counter reads the value entered in the R0 register and then it counts down the value at every pulse output. In-positioning is complete when the preset counter counts down to 0. The counting can be read at any time using the register read command.

By writing a specific start command, you can start the PCL5014 without letting the preset counter read the value entered in the R0 register.
The preset counter function is useful to let the PCL5014 output a remaining number of pulses if you stopped it on the way of in-positioning.

3.4.2 Ramping-down Point Counter

The ramping-down point counter is used for automatic start of deceleration in the varied-speed operation or in-positioning. The number of output pulses required for deceleration is calculated at the time of acceleration and the ramping-down point counter is set accordingly. The value is compared with that of the preset counter and when it equals to the latter, deceleration starts while at the same time the ramping-down point counter counts down.
You can read the counter value by writing the register read command.

3.5 Operation Mode Buffer and Control Mode Buffer

Basic operating conditions will be entered in the operation mode buffer and control mode buffer. You can set operating conditions by writing them from the CPU to addresses of operation mode buffer and can set control conditions by writing them from the CPU to addresses of control mode buffer.

3.5.1 Operation Mode Buffer

Write the following five conditions in the operation mode buffer:
(1) Operation mode (in-positioning, origin return, etc.)
(2) Moving direction
(3) $\overline{\pm SD}$ pin input valid/invalid
(4) Up/down counter ON/OFF
(5) Operation stop timing at either the stop of pulse output or the completion of a pulse cycle

3.5.2 Control Mode Buffer

Write the following eight conditions in the control mode buffer:
(1) Preset counter ON/OFF
(2) Whether the R5 value or an automatically calculated value is used as the starting point of deceleration in in-positioning
(3) Acceleration/deceleration mode—S-curve or linear
(4) Servomotor control $\overline{INP}$ pin input valid/invalid
(5) Automatic start of the next operation valid/invalid for in-positioning
(6) Input signal based simultaneous stop function valid/invalid
(7) Whether or not to output the simultaneous stop signal in an event of emergency stop due to the signal from the limit switch.
(8) Whether or not to effect the function to prevent such the abrupt change of pulse output rate as occurring if the preset number of output pulses lacks for in-positioning, which causes deceleration on the way of acceleration.

3.6 Operation Modes

The PCL5014 provides 13 operation modes. It operates in a selected mode, using conditions written in the operation mode buffer and based on parameters entered in registers.

3.6.1 Continuous Mode 1

The PCL5014 starts generating pulses upon receiving the start command and continues outputting pulses until receiving the stop command.

3.6.2 Continuous Mode 2

The PCL5014 outputs pulses in synchronization with signals input to PA and PB pins after receiving the start command until receiving the stop command. Use this mode if you wish to drive the motor manually through external pulse input.

3.6.3 Origin Return Mode 1

The PLC5014 stops outputting pulses when conditions for the completion of origin return are satisfied. The conditions are set in the R7 register (environment setting 2).

3.6.4 Origin Return Mode 2

The PCL5014 stops generating pulses upon outputting the number of pulses entered in the R0 register or when conditions for the completion of origin return are satisfied.

3.6.5 Origin Search Mode

After receiving the start command, the PCL5014 returns the axis to the origin from the designated direction while reciprocating the axis between plus and minus end limits.

3.6.6 Origin Escape Mode

This mode is used to let the axis escape from the origin despite the origin signal ON. The PCL5014 stops outputting pulses when conditions for the completion of origin escape are satisfied. The conditions are entered in the R7 register.

3.6.7 One-pulse Output Mode

The PCL5014 outputs only one pulse irrespective of the number of output pulses entered in the R0 register.

3.6.8 Timer Mode

This mode is to use the internal operation time as a timer. The internal operation is the same as the preset mode 1 below except for no pulse output in this mode.

3.6.9 Preset Mode 1

The PCL5014 puts the axis in position by outputting pulses to the number written in the R0 register. The moving direction is set in the operation mode buffer.

3.6.10 Preset Mode 2

The PCL5014 puts the axis in position by outputting pulses to the number written in the R0 register. The direction depends on a sign prefixed to the number.

3.6.11 Preset Mode 3

The PCL5014 moves the axis to an absolute position by using the up/down counter value. Regarding the up/down counter value as the present position and the R0 register value as the target position, the PCL5014 outputs pulses until the up/down counter value reaches the R0 register value.

3.6.12 Preset Mode 4

The PCL5014 puts the axis in position by outputting pulses in synchronization with signals input to PA and PB pins. This mode is similar to the continuous mode 2 except that the PCL5014 in this mode stops upon outputting pulses to the number written in the R0 register. This mode is useful to manually put the axis in position by inputting pulses through an external device.

3.6.13 Zero Return Mode

The PCL5014 outputs pulses until the up/down counter counts down to zero. The operation is the same as the preset mode 3 for which the target value is set at zero.

3.7 Control Functions

The PCL5014 provides sophisticated functions to control the motor in various ways.

3.7.1 Automatic Start of Next Operation

This function allows you to write parameters for the next operation in preregisters so that the PCL5014 can automatically start the next operation upon completing the present one. Writing parameters for the next operation during the present one in progress lets you eliminate a pause time between operations.

3.7.2 Microstep Control

Generally, with a microstep stepping motor driver a high in-positioning accuracy is ensured by stopping it at the full step position.

The PCL5014 performs the microstep control to stop microstep motor drivers with a resolution of up to 1/256 at their full step position. For example, if it is set for a microstep of 1/10, the PCL5014 can output 10 times the set number of output pulses.

3.7.3 Out-of-step Detection

The PCL5014 can detect an out-of-step status, provided that the stepping motor has a feedback encoder mounted. When it detects an out-of-step status, the PCL5014 stops outputting pulses.

3.7.4 Idling Pulse Output

The PCL5014 can initiate acceleration after outputting several pulses at the FL rate. This allows you to set the FL rate to a value near the upper limit of self-starting rate of the stepping motor.

3.7.5 Servomotor Interface

The PCL5014 provides the following servomotor control signals:

(1) $\overline{\text{INP}}$

The PCL5014 stops outputting pulses upon receiving this in-position signal.

(2) $\overline{\text{ERC}}$

The PCL5014 outputs this one-shot signal to clear the deviation counter of servomotor driver.

(3) $\overline{\text{ALM}}$

The PCL5014 stops outputting pulses upon receiving this alarm signal from the servomotor driver.

3.7.6 Manual Pulser Input

This function allows you to input pulses from the manual pulser to let the PCL5014 output corresponding pulses from $\overline{\text{OUT}}$ and DIR pins for manual operation of a device. From the pulser, the PCL5014 inputs plus and minus pulses or two 90° phase difference signals at PA and PB pins. The 90° phase difference signals can be multiplied.

3.7.7 Up/Down Counter

The up/down counter serves for present position control. It counts output pulses or signals input to EA and EB pins. Signals input to EA and EB pins are plus and minus pulses or 90° phase difference signals. Counted 90° phase difference signals may be multiplied signals.

3.7.8 Comparator

The PCL5014 provides two built-in comparator circuits for comparison of the counter value with parameters written in R10 and R11 registers. The subject counter may be the up/down counter or preset counter. When the result of comparison satisfies the comparing condition, the $\overline{\text{CMP}}$ pin is put at low level. If desired, you can program so that the PCL5014 stops outputting pulses when the comparing condition is satisfied.

3.7.9 Ouput Pulsewidth Control

You can control the output pulsewidth to make the stop timing earlier. When the output pulse rate is lower than the reference value, the pulsewidth is constant. But if the output pulse rate is higher than the reference value, the pulsewidth is 50% the duty cycle.

3.7.10 Simultaneous Start

With $\overline{\text{STA}}$ pins of multiple units of PCL5014 connected in cascade, you can simultaneously start all units of PCL5014 by writing the start signal to any of $\overline{\text{STA}}$ pins or inputting the start signal through an external circuit.

3.7.11 Simultaneous Stop

With $\overline{\text{STP}}$ pins of multinple units of PCL5014 connected in cascade, you can let the stop signal stop all units of PCL5014 simultaneously. The stop signal may be sent through an external circuit.

3.7.12 Dummy Operation

You can let the PCL5014 perform all activities except for pulse generation. This allows you to check the PCL5014 without running the machine.

3.7.13 Interrupt Signal Acceptable General-Purpose I/O Ports

The PCL5014 provides three pins of AP0 to AP2 as general-purpose I/O ports. If the CPU is interfaced with the 8-bit bus, pins D8 to D15 can also be used as general-purpose I/O ports of BP0 to BP7. Also, you can let pins AP0 to AP2 output an interrupt signal as required.

You can define these pins as input or output through the R6 register and can define their output status by commands or through the general-purpose I/O buffer (for BP pins only).

3.7.14 External Input Signals from Mechanical System

The PCL5014 can input the following position detecting signals from the mechanical system:

(1) $\overline{+\text{EL}}$ and $\overline{-\text{EL}}$ Signals

These are limit signals from the mechanical system. The PCL5014 stops outputting pulses immediately upon receiving the limit signal in the moving direction and keeps the stop condition even if the limit signal is turned off (except for the origin search mode).

(2) $\overline{+\text{SD}}$ and $\overline{-\text{SD}}$ Signals

These are deceleration signals from the mechanical system.. The PCL5014 decelerates to the FL rate upon receiving the deceleration signal in the moving direction during varied-speed operation in the continuous or origin return mode. When the deceleration signal is turned off, the PCL5014 accelerates to the FH rate, though the deceleration ON status may be latched.

(3) $\overline{\text{ORG}}$ Signal

This is the origin return signal from the mechanical system. The PCL5014 returns the mechanical system to the origin upon receiving this signal. The signal ON status may be latched.

3.7.15 Pulse Output Modes

The PCL5104 provides two pulse output modes. The common pulse mode lets it output the control pulse and direction pulse. The 2-pulse mode lets it output plus and minus pulses. You can change the output logic.

3.7.16 Interupt Signal Output

The PCL5014 can output the $\overline{\text{INT}}$ signal to the CPU based on any of 22 factors. It outputs the $\overline{\text{INT}}$ signal when stopped by the limit signal or other. Factors to initiate the $\overline{\text{INT}}$ signal also include conditions written in the R8 register. You can read the current interrupt factor as a status code. If two or more factors initiate the interrupt signal, you can read them in order of larger to smaller values. The $\overline{\text{INT}}$ signal is reset by reading status codes down to 0.

3.8 Monitor

Through designated addresses, you can read kinds of the current status of PCL5014.

3.8.1 Operation and Setting Status

(1) Operation status such as cessation of pulse output and deceleration
(2) Status of input/output pins
(3) Status of AP pins (general-purpose I/O ports)

3.8.2 Interrupt Status

Factors initiating the $\overline{\text{INT}}$ signal

3.8.3 General-Purpose I/O Port Status

Status of BP pins

3.8.4 Register Contents

Register contents and counter values can be read through the input/output buffer or the direct port (designated register contents or counter values only)

3.9 Basic Operation

The basic operation procedure is as follows:

3.9.1 Writing Operation Parameters

Write operation parameters from the CPU to the command buffer, operation mode buffer and control mode buffer.

3.9.2 Reading Status

Read status data from the status address to the CPU.

3.9.3 Writing Data to Registers

(1) Write register parameters from the CPU to proper addresses of the input/output buffer.

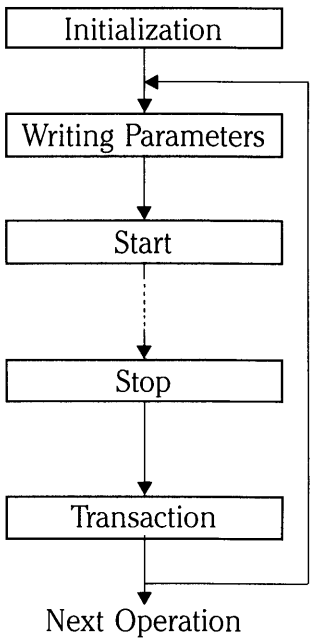
(2) Write the register write command to transfer register parameters from the input/output buffer to proper registers.

3.9.4 Reading Parameters from Registers

(1) Write the register read command to read the register parameter from the designated register to the input/output buffer.

(2) The CPU will read the register parameter from the address of the input/output buffer.

3.9.5 Typical Operation Procedure



Set the pulse output mode, external input signal logic, interrupt initiating factora, etc.

Write the number of output pulses, pulse rates, operation mode, etc.

Write the start command.

(Read data of position, pulse rate, etc.)

The PCL5014 stops outputting pulses with the stop command, upon completion of preset operation or with an external signal.

Take appropriate transactions such as reading interrupt factors.

4. Software

4.1 Address Map

The address map changes depending on the status of I/$\overline{M}$ pin so that the Intel CPU can access low-place data from a low-place address while the Motorola CPU can access high-place data from a low-place address.

4.1.1 Address Map with I/$\overline{M}$=L, B/$\overline{W}$=L (68000 or the equivalent)

	A3	A2	A1	A0	$\overline{US}$	Read Operation		Write Operation	
Word Access	H	H	H	L	L	Status	Bits 15 to 0	Command & operation mode buffers	
	H	H	L	L	L	Interrupt status		Control mode buffer	
	H	L	H	L	L	Input/output buffer	Bits 15 to 0	Input/output buffer	Bits 15 to 0
	H	L	L	L	L	Input/output buffer	Bits 31 to 16	Input/output buffer	Bits 31 to 16
	L	H	H	L	L	Direct port 1	Bits 15 to 0	(Invalid)	
	L	H	L	L	L	Direct port 1	Bits 31 to 16	(Invalid)	
	L	L	H	L	L	Direct port 2	Bits 15 to 0	(Invalid)	
	L	L	L	L	L	Direct port 2	Bits 31 to 16	(Invalid)	
Byte Access	H	H	H	L	H	Status	Bits 7 to 0	Command buffer	
	H	H	H	H	L	Status	Bits 15 to 8	Operation mode buffer	
	H	H	L	L	H	Interrupt status		Control mode buffer	
	H	H	L	H	L	(always 00HEX)		(Invalid)	
	H	L	H	L	H	Input/output buffer	Bits 7 to 0	Input/output buffer	Bits 7 to 0
	H	L	H	H	L	Input/output buffer	Bits 15 to 8	Input/output buffer	Bits 15 to 8
	H	L	L	L	H	Input/output buffer	Bits 23 to 16	Input/output buffer	Bits 23 to 16
	H	L	L	H	L	Input/output buffer	Bits 31 to 24	Input/output buffer	Bits 31 to 24
	L	H	H	L	H	Direct port 1	Bits 7 to 0	(Invalid)	
	L	H	H	H	L	Direct port 1	Bits 15 to 8	(Invalid)	
	L	H	L	L	H	Direct port 1	Bits 23 to 16	(Invalid)	
	L	H	L	H	L	Direct port 1	Bits 31 to 24	(Invalid)	
	L	L	H	L	H	Direct port 2	Bits 7 to 0	(Invalid)	
	L	L	H	H	L	Direct port 2	Bits 15 to 8	(Invalid)	
	L	L	L	L	H	Direct port 2	Bits 23 to 16	(Invalid)	
	L	L	L	H	L	Direct port 2	Bits 31 to 24	(Invalid)	

4.1.2 Address Map with I/$\overline{M}$=L, B/$\overline{W}$=H (6809 or the equivalent)

A3	A2	A1	A0	$\overline{US}$	Read Operation		Write Operation	
H	H	H	H	H	Status	Bits 7 to 0	Command buffer	
H	H	H	L	H	Status	Bits 15 to 8	Operation mode buffer	
H	H	L	H	H	Interrupt status		Control mode buffer	
H	H	L	L	H	Multi-purpose I/O buffer (BP7 to BP0)		Universal I/O buffer (BP7 to BP0)	
H	L	H	H	H	Input/output buffer	Bits 7 to 0	Input/output buffer	Bits 7 to 0
H	L	H	L	H	Input/output buffer	Bits 15 to 8	Input/output buffer	Bits 15 to 8
H	L	L	H	H	Input/output buffer	Bits 23 to 16	Input/output buffer	Bits 23 to 16
H	L	L	L	H	Input/output buffer	Bits 31 to 24	Input/output buffer	Bits 31 to 24
L	H	H	H	H	Direct port 1	Bits 7 to 0	(Invalid)	
L	H	H	L	H	Direct port 1	Bits 15 to 8	(Invalid)	
L	H	L	H	H	Direct port 1	Bits 23 to 16	(Invalid)	
L	H	L	L	H	Direct port 1	Bits 31 to 24	(Invalid)	
L	L	H	H	H	Direct port 2	Bits 7 to 0	(Invalid)	
L	L	H	L	H	Direct port 2	Bits 15 to 8	(Invalid)	
L	L	L	H	H	Direct port 2	Bits 23 to 16	(Invalid)	
L	L	L	L	H	Direct port 2	Bits 31 to 24	(Invalid)	

4.1.3 Address Map with I/$\overline{M}$=H, B/$\overline{W}$=L (8086 or the equivalent)

	A3	A2	A1	A0	$\overline{US}$	Read Operation		Write Operation	
Word Access	L	L	L	L	L	Status	Bits 15 to 0	Command & operation mode buffers	
	L	L	H	L	L	Interrupt status		Control mode buffer	
	L	H	L	L	L	Input/output buffer	Bits 15 to 0	Input/output buffer	Bits 15 to 0
	L	H	H	L	L	Input/output buffer	Bits 31 to 16	Input/output buffer	Bits 31 to 16
	H	L	L	L	L	Direct port 1	Bits 15 to 0	(Invalid)	
	H	L	H	L	L	Direct port 1	Bits 31 to 16	(Invalid)	
	H	H	L	L	L	Direct port 2	Bits 15 to 0	(Invalid)	
	H	H	H	L	L	Direct port 2	Bits 31 to 16	(Invalid)	
Byte Access	L	L	L	L	H	Status	Bits 7 to 0	Command buffer	
	L	L	L	H	L	Status	Bits 15 to 8	Operation mode buffer	
	L	L	H	L	H	Interrupt status		Control mode buffer	
	L	L	H	H	L	(always 00HEX)		(Invalid)	
	L	H	L	L	H	Input/output buffer	Bits 7 to 0	Input/output buffer	Bits 7 to 0
	L	H	L	H	L	Input/output buffer	Bits 15 to 8	Input/output buffer	Bits 15 to 8
	L	H	H	L	H	Input/output buffer	Bits 23 to 16	Input/output buffer	Bits 23 to 16
	L	H	H	H	L	Input/output buffer	Bits 31 to 24	Input/output buffer	Bits 31 to 24
	H	L	L	L	H	Direct port 1	Bits 7 to 0	(Invalid)	
	H	L	L	H	L	Direct port 1	Bits 15 to 8	(Invalid)	
	H	L	H	L	H	Direct port 1	Bits 23 to 16	(Invalid)	
	H	L	H	H	L	Direct port 1	Bits 31 to 24	(Invalid)	
	H	H	L	L	H	Direct port 2	Bits 7 to 0	(Invalid)	
	H	H	L	H	L	Direct port 2	Bits 15 to 8	(Invalid)	
	H	H	H	L	H	Direct port 2	Bits 23 to 16	(Invalid)	
	H	H	H	H	L	Direct port 2	Bits 31 to 24	(Invalid)	

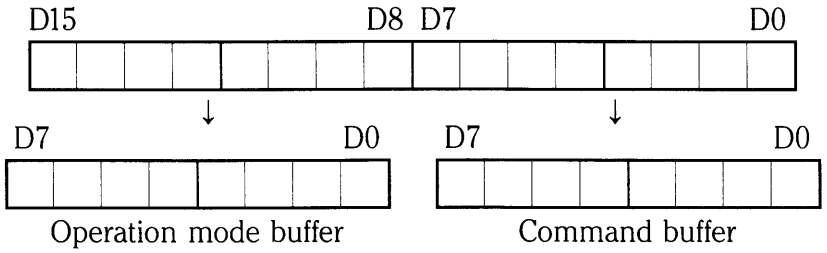
4.1.4 Address Map with I/$\overline{M}$=H, B/$\overline{W}$=H (Z80 or the equivalent)

A3	A2	A1	A0	$\overline{US}$	Read Operation		Write Operation	
L	L	L	L	H	Status	Bits 7 to 0	Command buffer	
L	L	L	H	H	Status	Bits 15 to 8	Operation mode buffer	
L	L	H	L	H	Interrupt status		Control mode buffer	
L	L	H	H	H	Universal I/O buffer (BP7 to BP0)		Universal I/O buffer (BP7 to BP0)	
L	H	L	L	H	Input/output buffer	Bits 7 to 0	Input/output buffer	Bits 7 to 0
L	H	L	H	H	Input/output buffer	Bits 15 to 8	Input/output buffer	Bits 15 to 8
L	H	H	L	H	Input/output buffer	Bits 23 to 16	Input/output buffer	Bits 23 to 16
L	H	H	H	H	Input/output buffer	Bits 31 to 24	Input/output buffer	Bits 31 to 24
H	L	L	L	H	Direct port 1	Bits 7 to 0	(Invalid)	
H	L	L	H	H	Direct port 1	Bits 15 to 8	(Invalid)	
H	L	H	L	H	Direct port 1	Bits 23 to 16	(Invalid)	
H	L	H	H	H	Direct port 1	Bits 31 to 24	(Invalid)	
H	H	L	L	H	Direct port 2	Bits 7 to 0	(Invalid)	
H	H	L	H	H	Direct port 2	Bits 15 to 8	(Invalid)	
H	H	H	L	H	Direct port 2	Bits 23 to 16	(Invalid)	
H	H	H	H	H	Direct port 2	Bits 31 to 24	(Invalid)	

NOTE: If you perform a read operation with the 16-bit data bus connected, the data buses which are not selected provide high impedance.

4.2 Word Access

If you use the 16-bit data bus, you can write a word in the command buffer, operation mode buffer and control mode buffer. In the case of 68000 CPU, a word written with A3=H, A2=H and A1=H is input as follows.



4.3 Read/Write from/to Registers

4.3.1 Writing Procedure

(1) Write data in the input/output buffer in a desired order.

(2) Write one of register write commands ($C0_{HEX}$ to CB_{HEX}, $D1_{HEX}$ to $D3_{HEX}$, $D7_{HEX}$ to DB_{HEX}) in the command buffer.

Precautions:
- To permit internal processing, do not write data or command for a time length of four cycles at the reference clock (approximately 0.2μs with a reference clock of 19.6608MHz).
- Also note that data and command written in preregisters R0 to R5, R15 and R16 during operation will be used for the next operation.

4.3.2 Reading Procedure

(1) Write one of register read commands (80_{HEX} to $8E_{HEX}$, 90_{HEX} to $9B_{HEX}$) to let the command buffer read register data.

(2) To permit internal processing, wait for a time length of four cycles at the reference clock (approximately 0.2μs with a reference clock of 19.6608MHz).

(3) Read data from the input/output buffer in a desired order.

NOTE: If the PCL5014 is interfaced with the CPU via the $\overline{WRQ}$ pin, the abovementioned waiting step is automatically processed.

4.4 Reading Status

Since the status at the start of processing for reading is latched, the data bus does not change during a read cycle. But if you want to continuously read the status, direct port 1 or 2, allow a time length of two or more cycles at the reference clock. If it is not secured, the previous data may be read out.

You can monitor the present operation status, the input/output status of $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{ORG}$, $\overline{CMP}$, $\overline{ALM}$, $\overline{ERC}$, $\overline{INP}$, and $\overline{CLR}$ signals and general-purpose I/P ports AP0 to AP2. The input/output status of $\overline{STA}$, $\overline{STP}$ and $\overline{EZ}$ signals can be read from registers R13 and R14.

4.5 Reading Interrupt Status

You can read the code for the factor which caused the $\overline{INT}$ signal. Reading this lets $\overline{INT}$ signal recover the high level.

4.6 Write/Read to/from General-Purpose I/O Ports BP7 to BP0

4.6.1 Writing

The status of the pin defined as output changes at the time of writing. The status of the pin defined as input is also stored in the output latch and it is output when the pin is re-defined as output. Writing "1" lets the corresponding output pin be high level. You can write a command to control bit by bit.

4.6.2 Reading

You can confirm the input/output status of each general-purpose I/O port. If the CPU interface is 16 bits, data of bits 7–0 are 0.

NOTE: Ports AP0 to AP2 are defined as input or output with the command.

4.7 Reading Data through Direct Ports 1 and 2

Without using a command, you can read the up/down counter value from the port 1.

Without using a command, you can read the value of any of the following four registers. Select the register by setting bits 9 and 8 of R7 as follows.

Bits of R7		Register Selected for Reading	Equivalent Command
9	8		
0	0	Preset counter	95HEX
0	1	R12: Counter monitor	8CHEX
1	0	R13: Command monitor 1	8DHEX
1	1	R14: Command monitor 2	8EHEX

The value is latched to the port when the lowest-place byte is read and unlatched from the port when the highest-place byte is read. So be sure to read data of all four bytes in the order from the lowest-place byte (word) to the highest-place byte (word).

When you read data through the direct port 1 or 2 then the status, allow a time length of two or more cycles at the reference clock. If such an allowance is not secured, the previous data may be read.

4.8 Default Conditions

Items	Default (Reset) Conditions
All internal registers	0
Command buffer	00_{HEX}
Operation mode buffer	00_{HEX}
Control mode buffer	00_{HEX}
Input/output buffer	00000000_{HEX}
$\overline{INT}$ pin	High level
Pins D0 to D7	High impedance
Pins D8 to D15	High impedance with B/$\overline{W}$ pin at low level Input pins with B/$\overline{W}$ at high level
$\overline{OUT}$ pin	High level
DIR pin	High level
$\overline{ERC}$ pin	High level
$\overline{WRQ}$ pin	High level
$\overline{BSY}$ pin	High level
Pins AP0 to AP2	Input pins
$\overline{FUP}$ pin	High level
$\overline{FDW}$ pin	High level
$\overline{CMP}$ pin	High level

4.9 Precautions in Designing Software

If you connect the PCL5014 to the CPU without using the $\overline{WRQ}$ output signal, allow a time length of four cycles at the reference clock between the following.

1) From writing a register read command (80_{HEX} to $9B_{HEX}$) to reading the data.
2) From writing a register write command ($C0_{HEX}$ to DB_{HEX}) to writing the next data
3) From writing a command to writing the next command.

Be sure to set preregisters at a value other than 0 and set the preregister R2 at a value higher than R1.

5. Operation

5.1 Setting Pulse Output Pattern

The PCL5014 provides three acceleration/deceleration modes.

(1) Linear Acceleration/Deceleration Mode

The PCL5014 is placed in this mode by setting bit 2 of control mode buffer at 0. In this mode the PCL5014 accelerates and decelerates the pulse output at a constant rate.

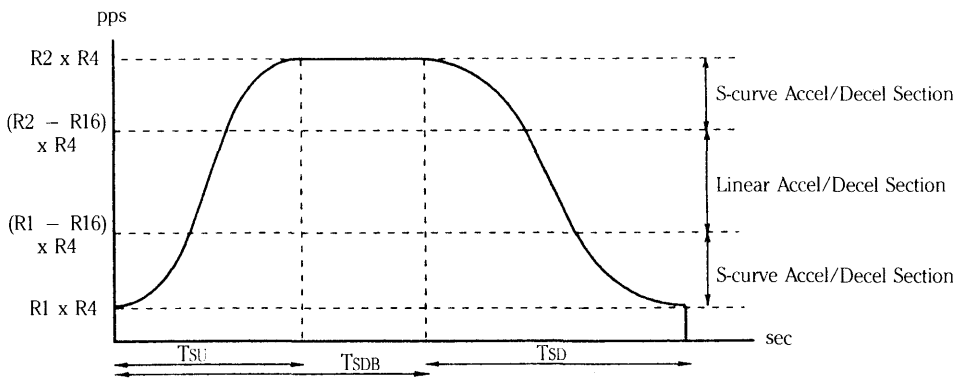
(2) S-curve Acceleration/Deceleration Mode with No Intermediate Linear Acceleration/Deceleration

The PCL5014 is placed in this mode by setting bit 2 of control mode buffer at 1 and with the R16 parameter at 0 or at a value higher than (R2 parameters − R1 parameter)/2. In this mode the PCL5014 accelerates and decelerates the pulse output while constantly varying the rate.

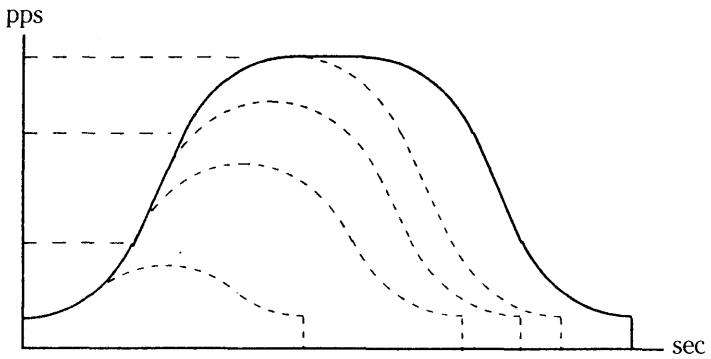
(3) S-curve Acceleration/Deceleration Mode with Intermediate Linear Acceleration/Deceleration

The PCL5014 is placed in this mode by setting bit 2 of control mode buffer at 1 and with the R16 parameter at other than 0 but lower than (R2 parameter − R1 parameter)/2. In this mode the PCL5014 performs S-curve acceleration/deceleration with an intermediate linear acceleration/deceleration on the way.

The pulse output pattern depends on parameters written in registers R1 to R5, R15 and R16. If the moving amount is small in the preset mode operation, the maximum rate is automatically lowered and smooth acceleration/deceleration is made. In such a case, the smaller the moving amount, the shorter the linear acceleration/deceleration section becomes and the S-curve section is not reduced unless the linear section is decreased to 0. (That is, if the PCL5014 is placed in the S-curve acceleration/deceleration mode with an intermediate linear acceleration/deceleration, no linear acceleration/deceleration is made for a smaller moving amount.)



Pulse Output Pattern with Acceleration/Deceleration



Automatic Adjustment of Maximum Rate Based on Moving Amount

Registers R1 to R5, R15 and R16 accompany preregisters. Write parameters to preregisters. The start signal lets the PCL5014 copy the parameters from preregisters to registers. If the parameters may be the same as previous, therefore, you need not write them anew.

When the parameters are read as 32-bit data, all high-place unused bits are 0.

5.1.1 Setting Pulse Rate Multiplication Factor

R4: Multiplication Factor Register, 12 bits

Write a multiplication factor in this register in a range of 1 to 4096 (FFF_{HEX}). R1 and R2 parameters are multiplied by the factor. The higher the multiplication factor, the coarser the pulse rate setting interval becomes. Usually, therefore, a smaller multiplication factor is used. Relations between a set value and multiplication factor are as follows:

$$\text{R4 parameter} = \frac{\text{Reference clock (Hz)}}{\text{(Multiplication factor) x 65536}} - 1$$

Examples with a reference clock of 19.6608MHz (Output pulse rate in pps)

Set Value	Multiplication	Output Pulse Rate	Set Value	Multiplication	Output Pulse Rate
2999 ($BB7_{HEX}$)	0.1	0.1 to 3276.7	59 ($3B_{HEX}$)	5	5 to 163835
599 (257_{HEX})	0.5	0.5 to 16383.5	29 ($1D_{HEX}$)	10	10 to 327670
299 ($12B_{HEX}$)	1	1 to 32767	14 ($0E_{HEX}$)	20	20 to 655340
149 (95_{HEX})	2	2 to 65534	5 (05_{HEX})	50	50 to 1638350
99 (63_{HEX})	3	3 to 98301	2 (02_{HEX})	100	100 to 3276700
74 ($4A_{HEX}$)	4	4 to 131068	1 (01_{HEX})	150	150 to 4915050

Setting example: Maximum rate = 50kpps → 2x mode → R4 = 149

5.1.2 Setting Starting Pulse Rate

R1: FL Rate Register, 15 bits

Write the starting pulse rate in this register in a range of 1 to 32,767 ($7FFF_{HEX}$). The rate is multiplied by the parameter written in the R4 register to be used for the constant speed operation at the FL rate or at the start/stop of varied-speed operation.

$$\text{R1 parameter} = \frac{\text{Starting pulse rate (pps)}}{\text{Multiplication factor}}$$

Setting example: 100 pps in 2x mode → R1 = 100/2 = 50

5.1.3 Setting Operating Pulse Rate

R2: FH Pulse Rate Register, 15 bits

Write the operating pulse rate in this register in a range of 1 to 32,767 ($7FFF_{HEX}$). The rate should be higher than what is written in the R1 register. The rate is multiplied by the parameter written in the R4 register to be used for the constant-speed operation at the FH pule rate or for the high-speed operation in the varied speed mode.

$$\text{R2 parameter} = \frac{\text{Operating pulse rate (pps)}}{\text{Multiplication factor}}$$

Setting example: 50 kpps in 2x mode → R2 = 50,000/2 = 25,000

5.1.4 Setting Maximum Acceleration Rate

R3: Acceleration Rate Register, 16 bits

Write the acceleration rate for the varied-speed operation in this register. The setting range is 1 to 65,535 ($FFFF_{HEX}$). If 0 is written in the R15 register, the rate written in the R3 register is used for deceleration. Relations of the R3 parameter with the maximum acceleration A_{SD} (pps/sec) and the acceleration time T_{SD} (sec) are as follows:

$$\text{R3 parameter} = \frac{\text{(Multiplication factor) x (Reference clock (Hz)}}{4 \text{ x } A_{SD}} - 1$$

Setting example: 100 kpps/sec in 2x mode →

R3 = (2 x 19660800)/(4 x 100000) − 1 = 97

5.1.5 Setting Maximum Deceleration Rate

R15: Deceleration Rate Register, 16 bits

Write the deceleration rate for the varied-speed operation in this register. The setting range is 1 to 65,535 ($FFFF_{HEX}$). If 0 (default) is written in the this register, the rate written in the R3 register is used for deceleration. Relations of the R15 parameter with the maximum deceleration A_{SD} (pps/sec) and the deceleration time T_{SD} (sec) are as follows, where A_{SD} is an absolute value of the negative deceleration rate:

$$\text{R15 parameter} = \frac{\text{(Multiplication factor) x (Reference clock (Hz)}}{4 \text{ x } A_{SD}} - 1$$

Setting example: 80 kpps/sec in 2x mode →

R15 = (2 x 19660800)/(4 x 80000) − 1 = 122

5.1.6 Setting S-curve Related Rate

R16: S-curve Related Rate Register, 14 bits

Write the S-curve related rate for the varied-speed operation in this register. The setting range is 1 to 16,383 ($3FFF_{HEX}$). S-curve acceleration/deceleration is applied between the FL pulse rate to the rate written in the R16 register and between (the FH pulse rate − the rate written in the R16 register) to the operating FH rate, while linear acceleration/deceleration is applied to the intermediate section.

If 0 (default) is written in this register, a value of (FH pulse rate − FL pulse rate)/2 is used for S-curve acceleration/deceleration and no linear acceleration/deceleration is applied. To put an intermediate linear acceleration/deceleration, write a value in a range of 1 to lower than (FH pulse rate − FL pulse rate)/2 in this register. Relations between the R16 parameter and S-curve related rate S are as follows.

$$\text{R16 parameter} = \frac{\text{S (pps)}}{\text{Mulfiplication factor}}$$

Setting example: If 1000 is written in the R16 register with an FL pulse rate of 100 pps (R1 = 50) and an FH pulse rate of 50 kpps (R2 = 25000) in 2x mode, the S-curve related rate is 2000. Thus, S-curve acceleration/deceleration is applied between 100 pps to 2100 pps and between 48000 pps to 50000 pps.

5.1.7 Acceleration/Deceleration Time

The acceleration/deceleration time is determined by parameters written in registers R1 to R4, R15 and R16 as follows:

(1) Linear Acceleration/Deceleration Mode

$$\text{Acceleration time } T_{SU} \text{ (sec)} = \frac{(R2 - R1) \times (R3 + 1) \times 4}{\text{Reference clock (Hz)}}$$

$$\text{Deceleration time } T_{SD} \text{ (sec)} = \frac{(R2 - R1) \times (R15 + 1) \times 4}{\text{Reference clock (Hz)}}$$

(2) S-curve Acceleration/Deceleration Mode with No Intermediate Linear Acceleration/Deceleration

$$\text{Acceleration time } T_{SU} \text{ (sec)} = \frac{(R2 - R1) \times (R3 + 1) \times 8}{\text{Reference clock (Hz)}}$$

$$\text{Deceleration time } T_{SD} \text{ (sec)} = \frac{(R2 - R1) \times (R15 + 1) \times 8}{\text{Reference clock (Hz)}}$$

(3) S-curve Acceleration/Deceleration Mode with Intermediate Linear Acceleration/Deceleration

$$\text{Acceleration time } T_{SU} \text{ (sec)} = \frac{(R2 - R1 + R16 \times 2) \times (R3 + 1) \times 4}{\text{Reference clock (Hz)}}$$

$$\text{Deceleration time } T_{SD} \text{ (sec)} = \frac{(R2 - R1 + R16 \times 2)) \times (R15 + 1) \times 4}{\text{Reference clock (Hz)}}$$

5.1.8 Setting Ramping-down Point

R5: Ramping-down Point Register, 24 bits

The ramping-down point is used for the varied-speed operation in the preset mode (in-positioning). Write the ramping-down point in this register in a range of 0 to 16,777,215 ($FFFFFF_{HEX}$).

You may use the automatic ramping-point setting function, which can be turned on or off by setting bit 1 of the control mode buffer. If it is turned on, the R5 parameter is offset from the automatic setting value. With the

automatic function turned on, the setting range is $-8{,}388{,}608$ (800000_{HEX+} to $+8{,}388{,}607$ ($7FFFFF_{HEX}$). A positive value initiates ramping-down earlier and a negative value initiates it later. If the automatic function is turned off, the ramping-down point written in the R5 register is used as it is.

A condition for normal operation of the automatic ramping-point setting function is:
(Time T_{SDB} from the start of acceleration at the FL pulse rate to the start of deceleration) $\geqq$ (Deceleration time T_{SD}). Generally, (R3 parameter) $\geqq$ (R15 parameter). Refer to "Acceleration/Deceleration Pattern" on page 21.

If you do not use the automatic ramping-down setting function, obtain the parameter to be written in the R5 register with the following procedure. Notice that with the automatic ramping-down setting function turned off, the automatic operating speed adjustment function too is turned off.

5.1.8.1 Ramping-down Point in Linear Acceleration/Deceleration Mode

(1) Check the trapezoidal pulse output pattern.
If the moving amount is too small, acceleration is not available to the FH pulse rate, thereby resulting in a triangular pattern. Use the following equation to ensure a trapezoidal pattern.

$$\text{(Minimum number of pulses required for trapezoidal pattern)} = \frac{(R2^2 - R1^2) \times (R3 + R15 + 2)}{(R4 + 1) \times 32768}$$

(2) Revise the FH pulse rate (R2).
If (R0) $\leqq$ (Minimum number of pulses required for trapezoidal pattern), the pulse output pattern is triangular. To make the pattern trapezoidal, revise the FH pulse rate (R2) using the following equation:

$$\text{Revised R2} \leqq \sqrt{\frac{R0 \times (R4 + 1) \times 32768}{R3 + R15 + 2} + R1^2}$$

(3) Write the ramping-down point in the R5 register.
For trapezoidal pulse output pattern:

$$R5 = \frac{(R2^2 - R1^2) \times (R15 + 1)}{(R4 + 1) \times 32768}$$

For triangular pulse output pattern:

$$R5 = \frac{R0 \times (R15 + 1)}{R3 + R15 + 2}$$

5.1.8.2 Ramping-down Point in S-curve Acceleration/Deceleration Mode with No Intermediate Linear Acceleration/Deceleration

(1) Check the trapezoidal pulse output pattern.
If the moving amount is too small, acceleration is not available to the FH pulse rate, thereby resulting in a triangular pattern. Use the following equation to ensure a trapezoidal pattern:

(Minimum number of pulses required for trapezoidal pattern) =

$$\frac{(R2^2 - R1^2) \times (R3 + R15 + 2)}{(R4 + 1) \times 16384}$$

(2) Revise the FH rate (R2).

If (R0) ≦ (Minimum number of pulses required for trapezoidal pattern), the pulse output pattern is triangular. To make the pattern trapezoidal, revise the FH rate (R2) using the following equation:

$$\text{Revised R2} \leqq \sqrt{\frac{R0 \times (R4 + 1) \times 16384}{R3 + R15 + 2} + R1^2}$$

(3) Write the ramping-down point in the R5 register.

$$R5 = \frac{(R2^2 - R1^2) \times (R15 + 1)}{(R4 + 1) \times 16384}$$

5.1.8.3 Ramping-down Point in S-curve Acceleration/Deceleration Mode with Intermediate Linear Acceleration/Deceleration

(1) Check the trapezoidal pulse output pattern.

If the moving amount is too small, acceleration is not available to the FH rate, thereby resulting in a triangular pattern. Use the following equation to ensure a trapezoidal pattern.

(Minimum number of pulses required for trapezoidal pattern) =

$$\frac{(R1 + R2) \times [(R16 \times 4) + (R2 - R1 - R16 \times 2)] \times (R3 + R15 + 2)}{(R4 + 1) \times 32768}$$

(2) Check availability of intermediate linear acceleration/deceleration.

If R0 ≦ (minimum number of pulses required for trapezoidal pattern), check availability of intermediate linear acceleration/deceleration.

(Minimum number of pulses required for intermediate linear acceleration/deceleration) =

$$\frac{(R1 + R16) \times R16 \times (R3 + R15 + 2)}{(R4 + 1) \times 4096}$$

(3) Revise the FH rate (R2).

If (minimum number of pulses required for intermediate linear acceleration/deceleration) < R0 ≦ (minimum number of pulses required for trapezoidal pattern), revise the FH rate (R2) to avoid a triangular pattern.

$$\text{Revised R2} \leqq -R16 + \sqrt{(R1)^2 + (R16)^2 - \times R0 \times R16 + \frac{R0 \times (R4 + 1) \times 32768}{R3 + R15 + 2}}$$

If R0 ≦ (minimum number of pulses required for intermediate linear acceleration/deceleration), write 0 in the R16 register to effect the S-curve acceleration deceleration mode with no intermediate linear acceleration/deceleration. Then follow the procedure of 5.1.8.2.

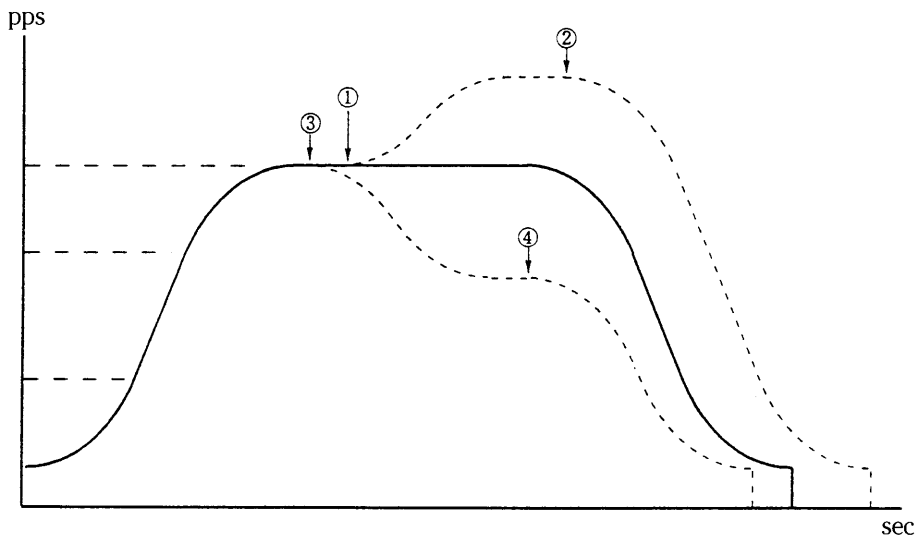
(4) Write the ramping-down point in the R5 register.

$$R5 = \frac{(R1 + R2) \times [(R16 \times 4) + (R2 - R1 - R16 \times 2)] \times (R15 + 1)}{(R4 + 1) \times 32768}$$

5.1.9 Changing Pulse Output Pattern during Operation

You can change the pulse rate and acceleration rate by revising the parameters written in registers R2, R3, R15 and R16. However, do not revise these parameters if the automatic ramping-down point setting function is made effective for the origin return mode 2, preset mode 1, 2 or 3 or zero return mode. If you revise, the automatic setting function is disabled to follow the parameters. For your reference, you can change pulse rates at a designated position using the comparator function.

Variations of Pulse Output Pattern in Preset Mode Operation



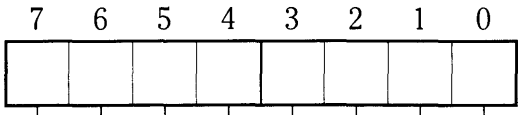
Example 1. ① The FH rate is revised to a higher one. (command D2HEX)
② Ramping-down starts automatically at the set ramping-down point.

Example 2. ③ The FH rate is revised to a lower one. (command D2HEX)
④ Ramping-down starts automatically at the set ramping-down point.

5.2 Operation and Control Mode Buffers

5.2.1 Operation Mode Buffer

The operation mode buffer has a prebuffer function to allow you to write parameters for the next operation during the present operation in progress.



Operation Mode
0000: Continuous mode 1
0001: Continuous mode 2
0010: Origin return mode 1
0011: Origin return mode 2
0100: Origin search mode
0101: Origin escape mode
0110: One-pulse output mode
0111: Timer mode
1000: Preset mode 1
1001: Preset mode 2
1010: Preset mode 3
1011: Zero return mode
1100: Preset mode 4

Moving Direction
0: Plus direction 1: Minus direction

$\overline{\pm SD}$ Signal Control
0: Valid 1: Invalid

Up/Down Counter
0: ON 1: OFF

Operation Completion Timing
0: A cycle at the output pulse rate is complete.
1: Output pulse is off.

(1) Operation Mode

Enter the 4-digit code to select a desired operation mode from 13.

(2) Moving Direction

Designate a desired moving direction by entering 0 or 1. Note, however, that the moving direction designated here is neglected in the continuous mode 2, preset modes 2 and 3 and zero return mode. With the plus direction selected, the up/down counter counts up.

(3) $\overline{\pm SD}$ Signal Control

Select whether or not to make the input to $\overline{+SD}$ and $\overline{-SD}$ pins valid. If this bit is set at 0, deceleration is made to the FL pulse rate when an $\overline{SD}$ signal in the moving direction is input during varied-speed operation. If the bit is set at 1, any $\overline{SD}$ signal is masked and does not cause deceleration. The setting condition of this bit has no relation with the $\overline{SD}$ input status on monitor.

(4) Up/Down Counter

If this bit is set at 1, the up/down counter stops operating. Set it at 1 when you need to operate without activating the up/down counter for the purpose of correcting backlash, etc. For your reference, the up/down counter does not count when the input signal is output pulse or in timer mode operation if the bit is set at 0.

(5) Operation Completion Timing

You can select a timing the PCL5014 stops outputting pulses. Set the bit at 0. The PCL5014 will stop outputting pulses when a cycle at the output pulse rate will be complete. Thus, you can secure a pause time if you restart immediately after stopping. Set the bit at 1. The PCL5014 will stop outputting pulses when an output pulse is off. Since the PCL5014 stops without waiting for completion of the cycle, you can shorten the cycle time if you do not restart immediately after stopping. (Refer to "5.4.9 Controlling Output Pulsewidth.')

Typical Settings vs. Operation Modes

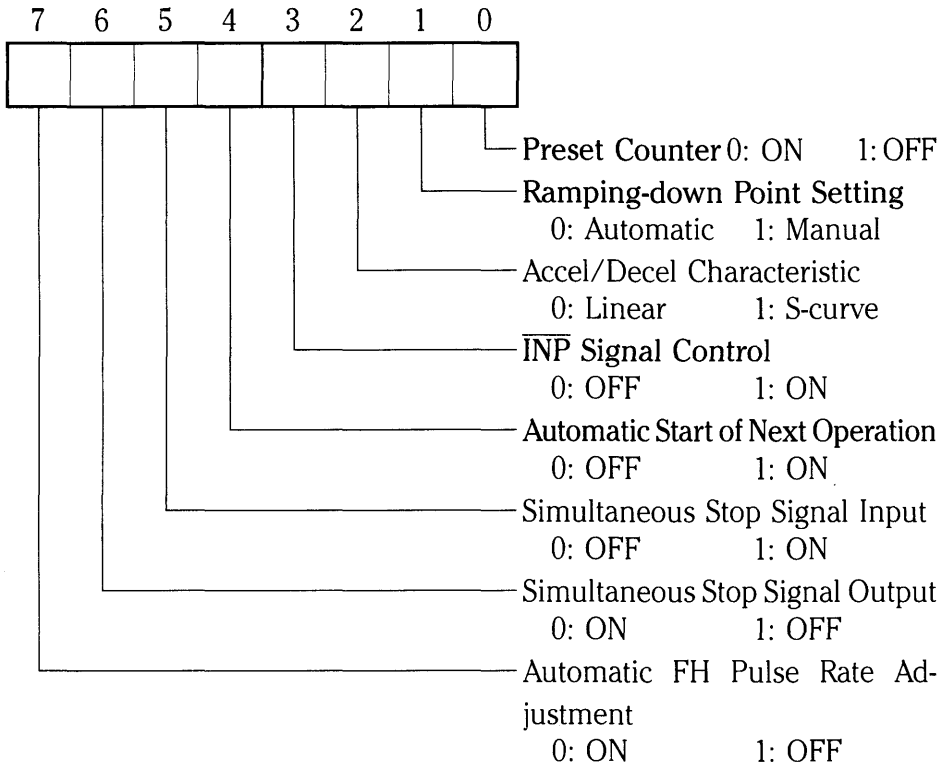
Settings									Operation Modes
7	6	5	4	3	2	1	0	HEX	
0	0	0	0	0	0	0	0	00	Continuous mode 1 in plus direction
0	0	0	1	0	0	0	0	10	Continuous mode 1 in minus direction
0	0	0	0	0	0	0	1	01	Continuous mode 2
0	0	0	0	0	0	1	0	02	Origin return mode 1 in plus direction
0	0	0	1	0	0	1	0	12	Origin return mode 1 in minus direction
0	0	0	0	0	0	1	1	03	Origin return mode 2 in plus direction
0	0	0	1	0	0	1	1	13	Origin return mode 2 in minus direction
0	0	0	0	0	1	0	0	04	Origin search mode in plus direction
0	0	0	1	0	1	0	0	14	Origin search mode in minus direction
0	0	0	0	0	1	0	1	05	Origin escape mode in plus direction
0	0	0	1	0	1	0	1	15	Orign escape mode in minus direction
0	0	0	0	0	1	1	0	06	One-pulse output mode in plus direction
0	0	0	1	0	1	1	0	16	One-pulse output mode in minus direction
0	0	0	0	0	1	1	1	07	Timer mode
0	0	0	0	1	0	0	0	08	Preset mode 1 in plus direction
0	0	0	1	1	0	0	0	18	Preset mode 1 in minus direction
0	0	0	0	1	0	0	1	09	Preset mode 2
0	0	0	0	1	0	1	0	0A	Preset mode 3
0	0	0	0	1	0	1	1	0B	Zero return mode
0	0	0	0	1	1	0	0	0C	Preset mode 4 in plus direction
0	0	0	1	1	1	0	0	1C	Preset mode 4 in minus direction
0	0	1	0	1	0	0	0	28	Preset mode 1 in plus direction*
0	1	0	0	1	0	0	0	48	Preset mode 1 in plus direction**
1	0	0	0	1	0	0	0	88	Preset mode 1 in plus direction***

*: with $\overline{\pm SD}$ signals invalid

**: with the up/down counter OFF

***: Completion timing at output pulse OFF

5.2.2 Control Mode Buffer



(1) Preset Counter

Set this bit at 1. The preset counter will stop counting down. Accordingly, if you operate the PCL5014 in the preset mode with this bit set at 1, the PCL5014 operates as in the continuous mode but stops outputting pulses when pulses are output in a set number from the time point you set it at 0 on the way of moving.

(2) Ramping-down Point Setting

If you start varied-speed operation by writing the 13HEX command in the origin return mode 2 or a preset mode, the PCL5014 starts ramping down the pulse output under the condition of (preset counter value) ≦ (ramping down point). Select the ramping-down point setting method by setting this bit at 0 or 1. If you set the bit at 0 (automatic mode), The R5 value is offset and the ramping-down point is the value obtained by adding the R5 value to the number of pulses required for acceleration. If you set the bit at 1 (manual mode), the R5 value is the ramping-down point.

(3) Accel/Decel Characteristic

Set this bit at 0 for a linear acceleration/deceleration pattern (constant acceleration/deceleration rate). Set it at 1 for an S-curve acceeration/deceleration pattern.

(4) $\overline{\text{INP}}$ Signal Control

If you use the PCL5014 to control a servomotor, the servomotor responds to pulses output from the PCL5014 with a delay and does not stop run-

ning when the PCL5014 completes the output of pulses. To stop the servomotor, you need to input the motor stop signal (in-position signal) which is output from the motor driver, to the $\overline{INP}$ pin. Set this bit at 1. Operation completion timing will be delayed to the time point the $\overline{INP}$ is input. Status, $\overline{BSY}$ and $\overline{INT}$ signals too will be delayed correspondingly.

(5) Automatic Start of Next Operation

Set this bit at 1. Upon completing the present operation, the PCL5014 will automatically start the next operation according to parameters written in preregisters. Note, however, that the PCL5014 does not automatically start the next operation unless preregisters are in the settled status at the time of completion of the present operation. The settled status indicates the condition where one of the following is satisfied.

- The start command for the next operation is written in.
- The settled status command (66HEX) is written in.

(6) Simultaneous Stop Signal Input

To stop multiple axes simultaneously, $\overline{STP}$ pins on all units of PCL5014 should be connected in cascade. If so required, you can electrically disconnect them by setting this bit at 0 so that the $\overline{STP}$ signal input may not simultaneously stop all units from generating pulses.

(7) Simultaneous Stop Signal Output

By setting this bit at 0, you can let the PCL5014 which stops due to an abnormal event, output the simultaneous stop signal from the $\overline{STP}$ pin to stop all other units.

(8) Automatic FH Pulse Rate Adjustment

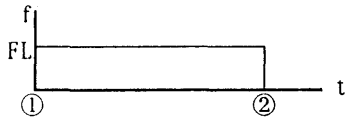
If the moving amount is too small in a preset mode, the automatic rammping-down point setting function lowers the FH pulse rate to avoid a triangular pulse output pattern. But you can make the automatic FH pulse rate adjustment function invalid by setting this bit at 1. If the ramping-down point is manually set, the automatic FH pulse rate adjustment is invalid irrespective of the status of this bit.

5.3 Operation Modes

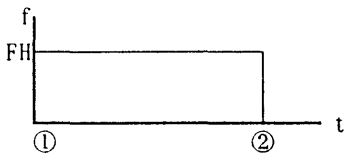
In any operation mode an $\overline{EL}$ signal in the moving direction stops the PCL5014 from outputting pulses. In varied-speed operation an $\overline{SD}$ signal in the moving direction lets the PCL5014 decelerate or stop pulse output after deceleration.

5.3.1 Continuous Mode 1

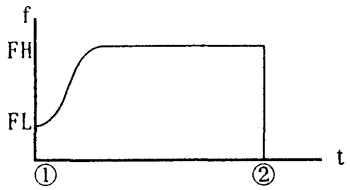
In this mode, writing the start command lets the PCL5014 output pulses in the direction set by bit 4 of the operation mode buffer until the stop command is written. The preset counter counts down referring to the value written in the R0 preregister.



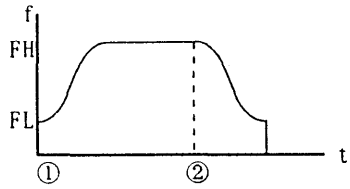
① Writing start command (10HEX) for constant speed operation at FL pulse rate
② Writing immediate stop command (09HEX)



① Writing start command (11HEX) for constant-speed operation at FH pulse rate
② Writing immediate stop command (09HEX)



① Writing start command (13HEX) for varied-speed operation
② Writing immediate stop command (09HEX)



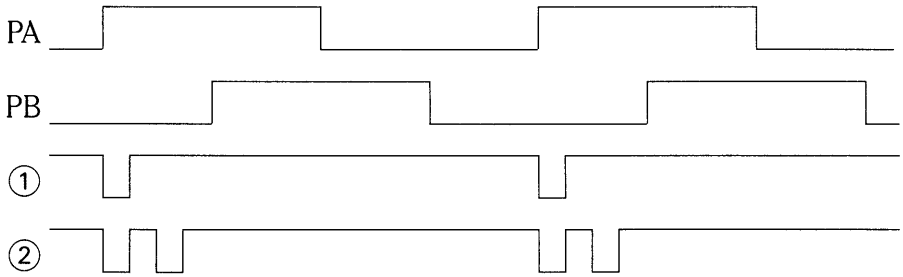
① Writing start command (13HEX) for varied-speed operation
② Writing deceleration stop command (0AHEX)

5.3.2 Continuous Mode 2

In this mode, external pulse signals (PA and PB) let the PCL5014 operate like in the continuous mode 1. For operation in this mode, you need to use the start command for varied-speed operation. You can control the number of output pulses and the pulse rate based on input PA and PB signals but the upper limit of pulse rate is the set FH pulse rate. The moving direction depends on PA and PB signals and the status of bit 4 of operation mode buffer is invalid.

When the PA and PB signals change simultaneously or when the pulse rate is beyond the limit, the PCL5014 outputs the $\overline{INT}$ signal. In such a case, the number of input pulses does not correspond to the number of output pulses. The preset counter counts down referring to the R0 preregister value. Refer to "5.4.6 Manual Pulser Input."

Operation with PA and PB pins given 90° phase difference signals multiplied by 1



① Output pulses with microstep control OFF
② Output pulses with microstep control set to 1/2

5.3.3 Preset Mode 1

In this mode you can place the axis in a desired position by designating the number of pulses and the direction. Write the number of output pulses in the R0 preregister and the moving direction in bit 4 of the operation mode buffer. The setting range for the R0 preregister is 0 to 268,435,445. The preset counter counts down referring to the R0 preregister value.

5.3.4 Preset Mode 2

In this mode you can place the axis in a desired position by designating the number of pulses with a signed value. Write the signed value (twos complement) in the R0 preregister. The moving direction is plus if the (+) sign is prefixed to the value and minus if the (−) sign is prefixed. The set status of bit 4 of the operation mode buffer is invalid. The setting range for the R0 preregister is −134,217,728 to +134,217,727. The preset counter counts down referring to the absolute value of R0 preregister.

5.3.5 Preset Mode 3

In this mode you can obtain an absolute movement with the up/down counter value as the present position. Set the target position by writing a positive or signed number in the R0 preregister, referring to the range of up/down counter selected by bit 28 of R5. The preset counter counts down with the absolute value of a difference between the R0 preregister value and the prevailing up/down counter value as the initial value. If you change the up/down counter value after starting, the number of output pulses does not change. Since the moving direction is automatically set, the set status of bit 4 of the operation mode buffer is invalid.

For example, if you start by writing "7000" in the R0 preregister with the up/down counter value at "15000," 8000 pulses are output in the minus direction. (7000 − 15000 = −8000)

5.3.6 Preset Mode 4

In this mode you can place the axis in a desired position in synchronization with input PA and PB signals. Designate the moving amount and direction with the same manner as for the preset mode 1. Input PA and PB signals let the PCL5014 output pulses like in the continuous mode 2 but the moving direction is as set by bit 4 of the operation mode buffer and has no relation with PA and PB signals. The preset counter counts down referring to the R0 preregister value.

5.3.7 Origin Return Mode 1

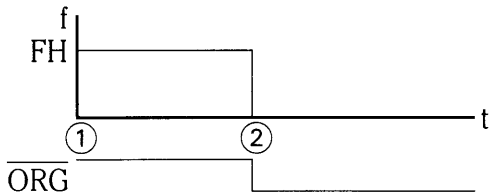
In this mode you can let the PCL5014 output pulses until the condition to complete the origin return is satisfied after writing the start command. The moving direction is as set by bit 4 of the operation mode buffer. If you set bit 6 of R7 at 1 in advance, the up/down counter will be reset upon completion of the origin return.

Select a condition to complete the origin return by setting bits 5–0 of R7 as follows.

(1) 00xxxx

The $\overline{\text{ORG}}$ signal stops the PCL5014 from outputting pulses. If the signal is on at the start, the PCL5014 outputs no pulse and completes the operation. (Bits 3–0 have no concern with this mode.)

In the case of setting 00xxxx

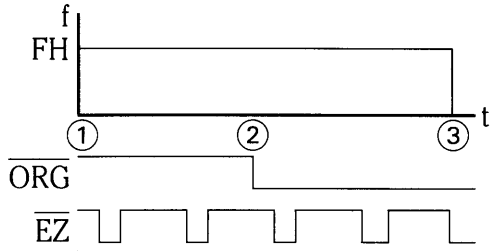


① Writing start command (11HEX) for constant-speed operation at FH pulse rate
② $\overline{\text{ORG}}$ signal ON

(2) 01nnnn

The (nnnn +1)th $\overline{\text{EZ}}$ signal after the $\overline{\text{ORG}}$ signal ON stops the PCL5014 from outputting pulses. To effect the origin return, the $\overline{\text{ORG}}$ signal should be ON during the time EZ signals are input in that number. If the $\overline{\text{ORG}}$ signal cannot be kept ON, you can internally latch the $\overline{\text{ORG}}$ signal by setting bit 30 of R6 at 1. if the $\overline{\text{ORG}}$ signal is ON at the start, the PCL5014 stops outputting pulses after the $\overline{\text{EL}}$ signals are counted to that number.

In the case of setting "010010"

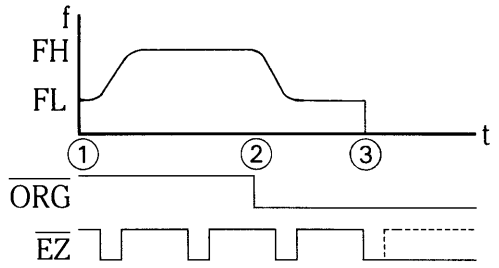


① Writing start command (11HEX) for constant-speed operation at FH pulse rate
② $\overline{ORG}$ signal ON
③ The 3rd $\overline{EZ}$ signal ON

(3) 10nnnn

The $\overline{ORG}$ signal which is turned on during varied-speed operation initiates deceleration and the (nnnn +1)th $\overline{EZ}$ stops the PCL5014 from outputting pulses. To effect the origin return, the $\overline{ORG}$ signal should be ON during the time EZ signals are input in that number. If the $\overline{ORG}$ signal cannot be kept ON during the time, you can internally latch the $\overline{ORG}$ signal by setting bit 30 of R6 at 1. If the $\overline{ORG}$ signal is ON at the start, the PCL5014 stops outputting pulses after the $\overline{EL}$ signals are counted to that number anew. The constant-speed operation shows the same effect as setting 01nnnn.

In the case of setting "100001"



① Writing start command (13HEX) for varied-speed operation
② $\overline{ORG}$ signal ON
③ The 2rd $\overline{EZ}$ signal ON

You can change the input logic of $\overline{ORG}$ signal with bit 5 of R6, and that of the $\overline{EZ}$ signal with bit 7 of R6. The preset counter counts down referring to the R0 preregister value.

6.3.8 Origin Return Mode 2

In this mode you can let the PCL5014 output pulses until the axis returns to the origin or pulses are output in a preset number. When started, the PCL5014 outputs pulses like in the origin return mode 1 but if the number of output pulses reaches the preset R0 preregister value before the origin return, it stops outputting pulses. Set the moving direction with bit 4 of the operation mode buffer. You can know the cause of stop, origin return or pulses output in a preset number, with the interrupt status code or by reading the preset counter value. Based on the preset counter value (read command 95HEX), you can know that pulses output in a preset number stopped the PCL5014 if the counter value is 0 and the origin return stopped the PCL5014 if the counter value is other than 0. If you want to judge the cause with an interrupt status code, you need to set bits 1 and 2 of R8 at 1 in advance. In this case, an interrupt status code of 02HEX indicates that pulses

output in a preset number stopped the PCL5014 and an interrupt status code of 03HEX indicates that the origin return stopped the PCL5014.

5.3.9 Origin Escape Mode

The $\overline{ORG}$ signal which is turned on does not always indicate that the axis returns to the origin. In such a case, you need to move the axis to a position which turns the $\overline{ORG}$ off, then return it to the origin. The origin escape mode allows you to move the axis to the position which turns the $\overline{ORG}$ signal off. Set the moving direction with bit 4 of the operation mode buffer.

Select a condition to complete the origin escape by setting bits 5–0 of R7 as in the case of the origin return.

(1) 00xxxx

The $\overline{ORG}$ which is turned off stops PCL5014 from outputting pulses. If the signal is off at the start, the PCL5014 does not output any pulse and completes the operation. (Bits 3–0 have no concern with the origin escape.)

(2) 01nnnn

The (nnnn +1)th $\overline{EZ}$ signal after the $\overline{ORG}$ turned off stops the PCL5014 from outputting pulses. The $\overline{ORG}$ signal should be off during the time $\overline{EZ}$ signals are input in that number. If the $\overline{ORG}$ signal is off at the start, the PCL5014 stops after $\overline{EZ}$ signals are counted to that number.

(3) 10nnnn

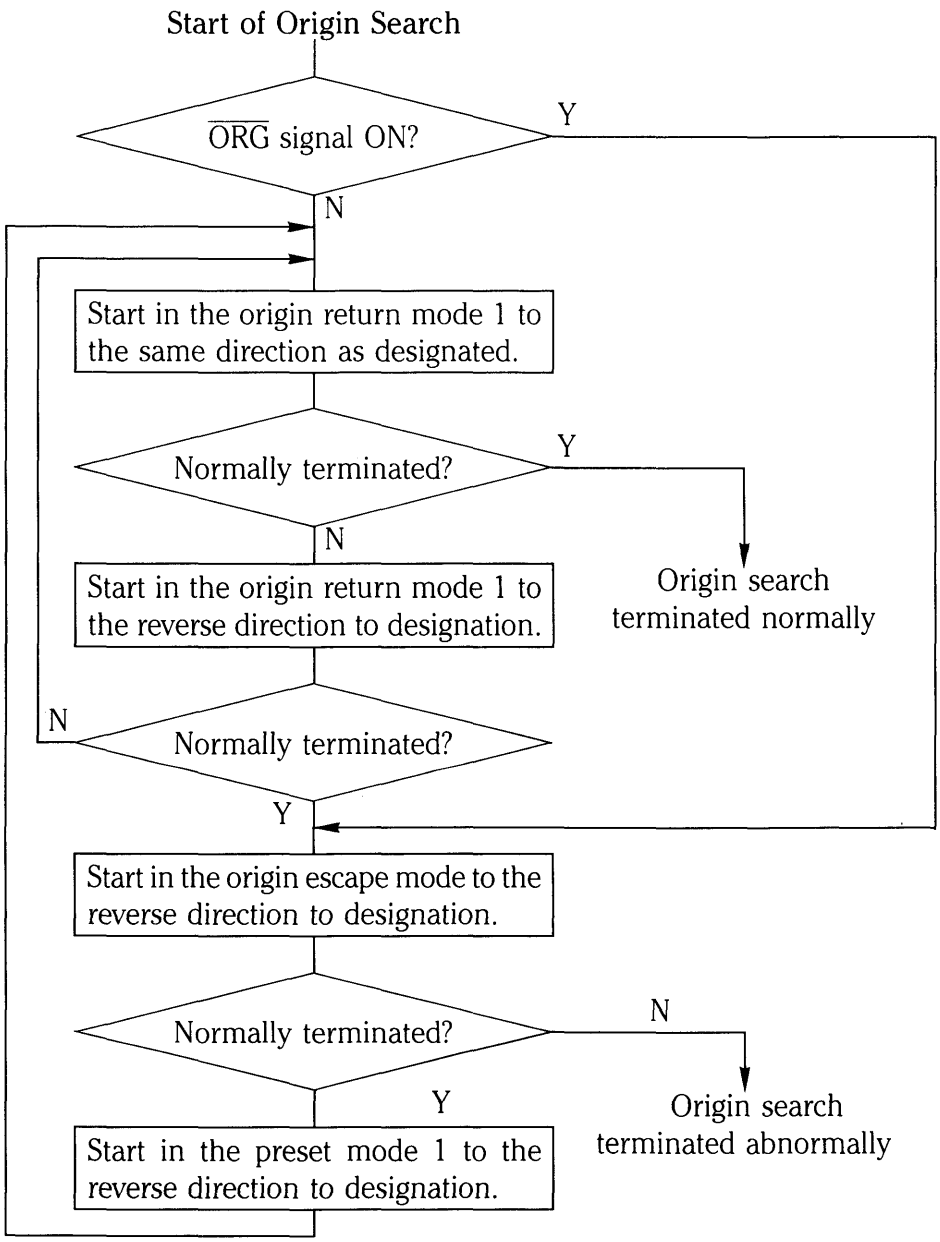
The $\overline{ORG}$ signal which is turned off during varied-speed operation initiates deceleration and the (nnnn +1)th $\overline{EZ}$ signal stops the PCL5014 from outputting pulses. To effect the origin escape, the $\overline{ORG}$ signal should be off during the time $\overline{EZ}$ signals are input in that number. If the $\overline{ORG}$ signal is on at the start, the PCL5014 stops after $\overline{EZ}$ signals are counted to that number anew. In the constant-speed operation, this setting provides the same operation as "01nnnn."

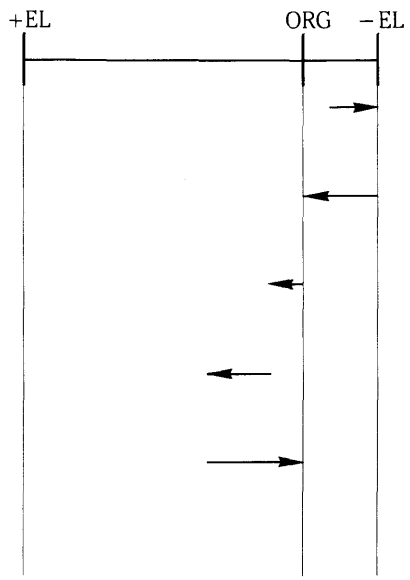
You can change the input logic of $\overline{ORG}$ signal with bit 5 of R6 and that of $\overline{EZ}$ signal with bit 7 of R6. The preset counter counts down referring to the R0 preregister value.

5.3.10 Origin Search Mode

In this mode you can return the axis to the origin from a designated direction after reciprocating it between $+\overline{EL}$ and $-\overline{EL}$. Set the moving direction with bit 4 of the operation mode buffer. Internal operation is a series of movements in multiple modes.

If you set bit 29 of R6 at 1 so that the $\overline{SD}$ signal which is turned on initiates deceleration then stops the PCL5014 from outputting pulses, the effect is the same as with the $\overline{EL}$ signal ON.





Operation of origin search executed in minus direction from between ORG and −EL

(1) The axis starts moving in the minus direction as designated (origin return mode 1 to the same direction).
(2) $\overline{-EL}$ signal stops the axis then lets it move to the reverse direction (+) to designation. (Origin return mode 1 to the reverse direction)
(3) $\overline{ORG}$ signal stops the axis then moves it to the origin escape position so that it may return to the origin from the designated direction. (Origin escape mode to reverse direction)
(4) The axis moves further in the plus direction so that the $\overline{ORG}$ signal is securely turned off. (Preset mode 1 to the reverse direction)
(5) The axis starts moving in the designated minus direction. (Origin return mode 1 in the same direction)
(6) The axis stops at the origin.

5.3.11 One-pulse Output Mode

In this mode you can let the PCL5014 output only one pulse (or pulses in a unit number if the microstep control is used). Set the moving direction with bit 4 of the operation mode buffer. Operation in this mode is the same as in the preset mode 1 with 1 written in the R0 preregister. But you need not write 1 in the R0 preregister. The preset counter counts down referring to 1.

5.3.12 Timer Mode

This mode allows you to use the PCL5014 as a timer referring to internal operation time with no pulse output. Internal operation is the same as in the preset mode 1. $\overline{EL}$ and $\overline{SD}$ signals are invalid (always regarded as OFF). In the timer mode, the up/down counter stops counting if the input is the output pulse. If the output pulse is used as a common pulse to output a direction signal from the DIR pin, the status of DIR pin changes according to bit 4 of the operation mode buffer. The start command is regarded as a start signal for the constant-speed operation and the internal operation time is the product of a cycle of output pulses and the R0 preregister value (e.g. 1000 pps x 120 pulses (R0 preregister value) = 120ms). Irrespective of the status of bit 3 of the control mode buffer, the $\overline{INP}$ signal does not delay the completion of operation. The preset counter counts down referring to the R0 preregister value.

To eliminate error of the internal operation time, set bit 7 of the operation mode buffer at 0 so that the operation completion timing is at the completion of a cycle of output pulses.

5.3.13 Zero Return Mode

In this mode in-positioning is made so that the up/down counter counts down to zero at the completion of operation. The effect is the same as if you set the R0 preregister at 0 in the preset mode 3 but you can omit setting of the R0 preregister. The preset counter counts down with the absolute value of up/down counter as the initial value. If the up/down counter value is revised after starting, the number of output pulses does not change. The moving direction is automatically set, thereby making the status of bit 4 of the operation mode buffer invalid.

5.4 Control Functions

5.4.1 Automatic Start of Next Operation

You can write parameters during operation in progress to automatically start the next operation according to newly set parameters. To effect such the automatic start function, set bit 4 of the control mode buffer at 1. This function allows you to eliminate a pause time between operations.

You can write parameters in the following preregisters and prebuffers, 10 in total.

R0 preregister [number of output pulses (moving amount)]
R1 preregister (FL pulse rate)
R2 preregister (FH pulse rate)
R3 preregister (acceleration rate)
R4 preregister (multiplication factor)
R5 preregister (ramping-down point)
R15 preregister (deceleration rate)
Operation mode prebuffer
Command prebuffer (start command only)

To prevent the PCL5014 from starting the next operation based on old parameters in the case where the present operation is terminated before parameters for the next operation are written completely, we designed the PCL5014 so that it checks whether or not parameters for the next operation are settled. If preregisters are not placed in a settled status at the completion of the present operation, the PCL5014 does not start the next operation automatically. The PCL5014 is placed in an unsettled status by writing the register unsettled command or if the start command for the next operation is not written in.

The settled status indicates that any of the following two conditions is satisfied:

(1) The start command for the next operation is written in.
(2) The settled status command (66HEX) is written in.

If the present operation was stopped due to an abnormal event or by writing a command, the next operation does not start automatically. Accordingly, in the continuous mode 1 or 2 in which you need to write a command to stop the operation, you cannot use these preregisters to start the next operation automatically.

The PCL5014 stops outputting pulses if any of the following occurs.

(1) $\overline{\text{EL}}$ signal is turned on in other than the origin search mode.
(2) $\overline{\text{SD}}$ signal is turned on in other than the origin search mode.
(3) $\overline{\text{ALM}}$ signal is turned on.
(4) Out-of-step is detected.
(5) Comparator condition is satisfied.
(6) $\overline{\text{STP}}$ signal is input.
(7) Immediate stop command (09HEX) is written in.
(8) Deceleration stop command (0AHEX) is written in.
(9) Emergency stop command (63HEX) is written in.

By reading R14, you can check the settled status for the next operation.

(1) Bit 16 is '1' if a parameter is written in the R0 preregister and '0' when started.

(2) Bit 17 is '1' if a parameter is written in the R1 preregister and '0' when started.

(3) Bit 18 is '1' if a parameter is written in the R2 preregister and '0' when started.

(4) Bit 19 is '1' if a parameter is written in the R3 preregiser and '0' when started.

(5) Bit 20 is '1' if a parameter is written in the R4 preregister and '0' when started.

(6) Bit 21 is '1' if a parameter is written in the operation mode prebuffer and '0' when started.

(7) Bit 22 is '1' if parameters for the next operation are settled and '0' if they are not settled.

(8) Bit 24 is '1' if a parameter is written in the R5 preregister and '0' when started.

(9) Bit 25 is '1' if a parameter is written in the R15 preregister and '0' when started.

(10) Bit 26 is '1' if a parameter is written in the R16 preregister and '0' when started.

If parameters for the next operation are the same as for the present operation, you need not write them anew. If you set bit 14 of R8 at 1, the $\overline{\text{INT}}$ signal is output at the start of next operation, thereby allowing you to get the timing for writing parameters for the succeeding operation.

- To make the automatic start of next operation valid/invalid
  Set bit 4 of the control mode buffer at—
  0: to turn the function ON
  1: to turn it OFF

- To place preregisters in settled status:
  (1) Write the start command for the next operation in the command buffer (the start command will be the same as used for the present operation), or
  (2) Write the settled status command 66HEX to the command buffer.

- Preregisters are placed in unsettled status:
  (1) When an abnormal event stops the PCL5014 or when a command is written to the command buffer, or
  (2) When the unsettled status command 67HEX is written to the command buffer.

- To check preregister status
  Read bit 22 of R14:
  0: Unsettled status
  1: Settled status
- To output the $\overline{\text{INT}}$ signal at the start of next operation
  Set bit 14 of R8 at 1.
- To check the interrupt factor at the start of next operation
  Read the interrupt status. If the interrupt status code is 14HEX at the INT signal output, it indicates that the next operation is ready for starting and preregisters can accept new parameters.

5.4.2 Microstep Control

You can perform microstep control to suppress the step vibration of stepping motor. Use of a microstep driver may suppress the step vibration but the positioning accuracy is not ensured unless it stops at a full-step position. The PCL5014 has a function to stop the motor at a full-step position. Furthermore, the R0 register (preset amount), the up/down counter (R9) and R10 and R11 registers (comparator data) use the number of full steps irrespective of the microstep control.

Resolution of microstep is $1/n$ (n is available in a range of 1 to 256). Set bits 31–24 (unit number of output pulses) of R7 at (n − 1) to determine a resolution. If it is set at 0, the resolution is 1/1 (= full step). The output frequency is the same as in the case the microstep control is not used. If the PCL5014 is operated in the preset mode 1 with the resolution set at 1/10 (set value = 9) and R0 set at 12, the PCL5014 outputs 120 pulses to change the present position by 12 counts.

Under the microstep control, the PCL5014 stops after outputting pulses in the unit number and does not stop on the way. However, the emergency stop command, soft reset command or $\overline{\text{RST}}$ signal stops the PCL5014 at other than full-step position. Also, by writing a microstep control range in the R7 register, you can let the $\overline{\pm\text{EL}}$ signal, $\overline{\text{ALM}}$ signal or completion of origin return stop the PCL5014 immediately in other than full-step position. Such the operation is useful to control the motor in some number of units and not for the purpose of microstep. (e.g. to control the machine which moves by 0.2μm per pulse, in a unit of 1μm)

- To set the unit number of output pulses for the microstep control
  Write a value of (resolution of microstep − 1) in bits 31 to 24 of R7. The setting range is 0 to 255.
- To set the microstep control range
  Set bit 23 of R7 at—
  0: Microstep control at all times
  1: No microstep control at the stop initiated by the $\overline{\text{EL}}$ signal, $\overline{\text{ALM}}$ signal or completion of origin return.

- Emergency stop command
  Write the command 63HEX to the command buffer. The PCL5014 will immediately stop even in other than full-step position and output the $\overline{ERC}$ signal as a one-shot signal.

5.4.3 Out-of-step Detection

The PCL5014 is equipped with a 6-bit deviation counter to detect an out-of-step status of stepping motor. Mount a feedback encoder onto the stepping motor. The deviation counter will count a deviation between command pulses and pulses fed back from the encoder and if the value exceeds a certain level (maximum deviation: 1 to 31), the PCL5014 will judge an out-of-step status and stop generating pulses while outputting the $\overline{INT}$ signal. The encoder should have the same resolution as the stepping motor (or a resolution of full step under the microstep control).

This detection function is effective whether the motor is operating or not. So you can detect a deviation due to an external force applied during suspension. Set bits 12–8 of R8 at a maximum deviation which will be compared with the deviation counter value. If you set these bits at 00000 (default), the out-of-step detection function is deactivated.

The encoder mounted onto the stepping motor feeds back plus and minus pulses or 90° phase difference signals to ERA and ERB pins. 90° phase difference signals multiplied by 1, 2 or 4 may be counted. Select the input mode with bits 15 and 14 of R6. A simultaneous change of ERA and ERB input status causes an error, thereby letting the PCL5014 output the $\overline{INT}$ signal.

You can read the value of the deviation counter for out-of-step detection throuh the R12 register and reset it by writing the deviation counter clear command.

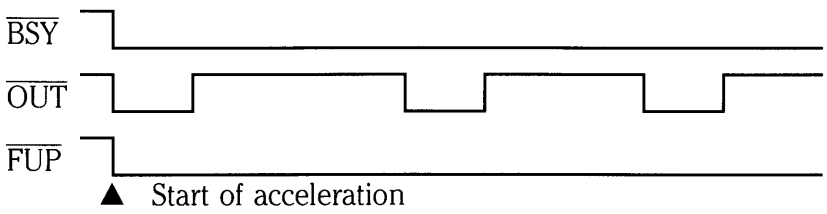
- Deviation counter value for out-of-step detection
  Write a maximum deviation value in bits 12 to 8 of R8. The setting range is 0 to 31. When the PCL5014 detects an out-of-step status, it immediately stops outputting pulses while outputting the $\overline{INT}$ signal.
- ERA/ERB input mode
  Set bits 15 and 14 of R6 to—
  00: 90° phase difference signals in 1x mode
  01: 90° phase difference signals in 2x mode
  10: 90° phase difference signals in 4x mode
  11: Plus and minus pulses
- Interrupt status code for out-of-step detection
  The interrupt status code 0CHEX indicates that the $\overline{INT}$ signal was initiated by out-of-step detection (interrupt initiating factor = bits 12 to 8 of R8 $\neq$ 0).

- Deviation counter value for out-of-step detection
  You can read the 6-bit counter value with a plus or minus sign in extended 8 bits through bits 31 to 24 of R12. If it is a minus value, it is a twos complement. When the motor is in a minus position from the integrated position, the value is positive.
- Command to clear the deviation counter for out-of-step detection
  Write the 62HEX to the command buffer.
- Interrupt status code for ERA/ERB input error
  The interrupt status code 13HEX indicates that the $\overline{INT}$ signal was initiated due to simultaneous change of ERA and ERB input signals (interrupt initiating factor: bits 12 to 8 of R8 $\neq$ 0).

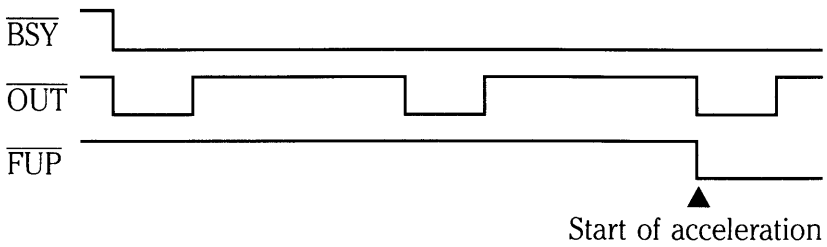
5.4.4 Idling Pulse Output

Usually, in the varied-speed operation the PCL5014 starts acceleration upon outputting the first pulse. Using the idling pulse output function, you can let the PCL5014 initiate acceleration after outputting several pulses at the FL pulse rate. If you do not use this function, the first pulse cycle is shorter than that of the set FL pulse rate because acceleration starts upon output of the first pulse. Due to this, the pulse rate at the start of accleration is higher than the set FL pulse rate. If you use the idling pulse output function, the timing to initiate acceleration is delayed by the set number of idling pulses, thereby making the initial rate the FL pulse rate and allowing you to set the FL pulse rate at a rate near the upper limit of self-starting rate of stepping motor. Set a desired number of idling pulses with bits 14–12 of R7. If you set it at n (n = 1 to 7), the nth pulse provides the timing for acceleration. Setting at 0 results in the same effect as setting at 1. With the microstep control function used, the PCL5014 starts acceleration after outputting idling pulses to the number of (n x unit number of output pulses).

In the case of n = 0 or 1



In the case of n = 3



- Number of idling pulses
  Write a desired number of idling pulses in bits 14 to 12 of R7. The setting range is 0 to 7. The PCL5014 will start acceleration after outputting pulses to that number at the FL pulse rate.
- You can read the idling pulse counter value through bits 22 to 20 of R12.

5.4.5 Servomotor Interface

The PCL5014 provides the following three signals for servomotor control.

(1) $\overline{\text{INP}}$

Usually, a pulse train input servomotor driver has a deviation counter built in to detect a deviation between input command pulses and feedback pulses. Theoretically, the servomotor operates with some delay from command pulses. Accordingly, if the pulse generator stops outputting pulses, the servomotor does not stop running until the deviation counter recovers the zero status. When the counter recovers the zero status, the servo driver outputs the in-position signal to the pulse generator to indicate the motor stops running. The $\overline{\text{INP}}$ pin inputs this in-position signal.

Usually, the PCL5014 stops generating pulses upon completion of outputting pulses as designated. But by setting bit 3 of the control mode buffer at 1, you can delay the completion of operation to the time when the $\overline{\text{INP}}$ signal is turned on. Status, $\overline{\text{BSY}}$ and $\overline{\text{INT}}$ signals are also delayed. However, the $\overline{\text{EL}}$ or $\overline{\text{ALM}}$ signal or the completion of origin return does not cause the $\overline{\text{INP}}$ signal to delay the timing of completion. The $\overline{\text{INP}}$ signal may be a pulse signal, of which the shortest width is 64 cycles at the reference clock (3μs with a clock frequency of 19.6608MHz). By turning the external input filter off, you can make the pulsewidth two cycles at the reference clock (0.1μs with a reference clock of 19.6608MHz).

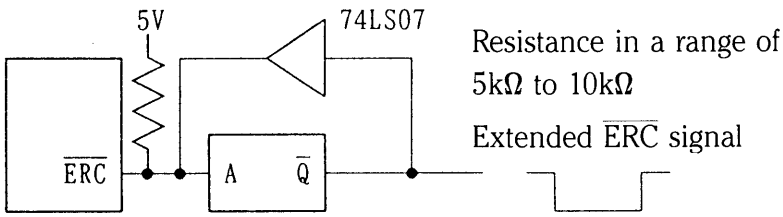
- To let the PCL5014 delay the completion of pulse output until receiving $\overline{\text{INP}}$ signal
  Set bit 3 of the control mode buffer at 1.
  The PCL5014 will delay the completion of pulse output until the $\overline{\text{INP}}$ signal is on. But the $\overline{\text{EL}}$ signal, $\overline{\text{ALM}}$ signal or origin return will stop the PCL5014 immediately without any delay.
- To select the $\overline{\text{INP}}$ signal input logic
  Set bit 3 of R6 at—
  0: negative logic
  1: positive logic

- Reading $\overline{INP}$ pin status
  Read bit 1 of status.
  0: $\overline{INP}$ pin OFF
  1: $\overline{INP}$ pin ON
- External input signal filter
  Set bit 8 of R6 at—
  0: Minimum pulsewidth is 64 cycles at the reference clock
  1: OFF

(2) $\overline{ERC}$

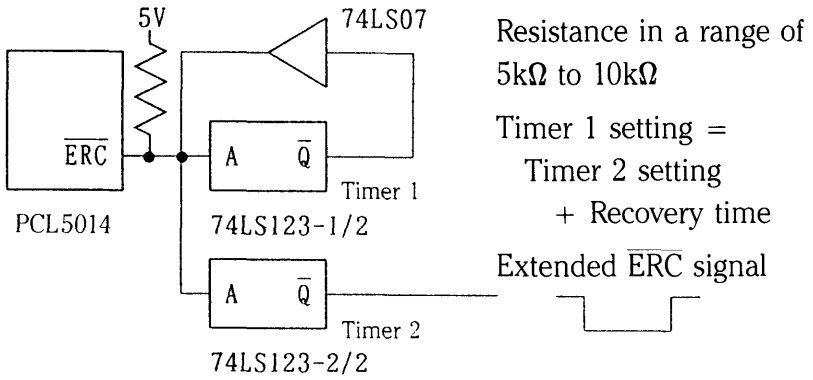
Since the servomotor operates with some delay from pulses generated from the PCL5014, it keeps operating by responding to pulses remaining in the deviation counter of the driver if the $\overline{EL}$ signal or the completion of origin return stops the PCL5014 from outputting pulses. The $\overline{ERC}$ signal allows you to immediately stop the servomotor by resetting the deviation counter to zero. The $\overline{ERC}$ signal is output as a one-shot signal. The pulsewidth is a time length of 4096 cycles at the reference clock (approximately 200μs with a reference clock of 19.6608MHz). Writing the emergency stop command lets the PCL5014 output the $\overline{ERC}$ signal. By setting bit 9 of R6 at 1, you can let the $\overline{EL}$ signal, the completion of origin return or $\overline{ALM}$ signal output the $\overline{ERC}$ signal to immediately stop the servomotor.

Some servo drivers require the $\overline{ERC}$ signal to have a time width of 200μs or longer. If you make such connection that the extended signal by a one-shot IC or the like is fed back to the $\overline{ERC}$ pin through an open collector output (TTL 7407 or the like), the timing of starting the timer to let the $\overline{ERC}$ recover the OFF status is delayed and the status monitor provides the pulsewidth extended signal.



Take care that the servo driver may not immediately accept command pulses if the $\overline{ERC}$ signal recovers the OFF status. By setting bit 10 of R7 at 1, you can delay the start by 4096 cycles at the reference clock (approximately 200μs with a reference clock of 19.6608MHz) from writing the start command after the $\overline{ERC}$ signal recovers the OFF status.

If a time length of over 200μs is required for the $\overline{ERC}$ signal to recover the OFF status, connect two timers as shown below.



- Automatic output of $\overline{ERC}$ signal
  Set bit 9 of R6 at 1. The $\overline{ERC}$ signal will be automatically output when $\overline{EL}$ signal, $\overline{ALM}$ signal or origin return stops the PLC5014 from outputting pulses.
- $\overline{ERC}$ signal OFF timer
  Set bit 10 of R7 at 1. The PCL5014 will start with a delay of 4096 cycles at the reference clock.
- Reading ERC signal status
  Read bit 10 of status.
  0: $\overline{ERC}$ signal OFF
  1: $\overline{ERC}$ signal ON

(3)$\overline{ALM}$

The $\overline{ALM}$ pin receives the alarm signal output from the servo driver. The signal immediately stops the PCL5014 from generating pulses. You can change the input logic by setting the R6 register. Whether or not the PCL5014 is generating pulses, the $\overline{ALM}$ signal lets it output the $\overline{INT}$ signal. If the $\overline{ALM}$ signal is in the ON status at the start, the PCL5014 outputs the $\overline{INT}$ signal without generating any command pulse. The $\overline{ALM}$ signal may be a pulse signal, of which the shortest width is a time length of 64 cycles at the reference clock (3μs with a reference clock of 19.6608MHz). By turning the external input filter off (setting bit 8 of R6 at 1), you can make the pulsewidth 2 cycles at the reference clock (0.1μs with a reference clock of 19.6608MHz).

- ALM signal input logic
  Set bit 6 of R6 at—
  0: Negative logic
  1: Positive logic
- Interrupt status code for $\overline{ALM}$ signal
  The interrupt status code 0B$_{HEX}$ indicates that the $\overline{ALM}$ signal initiated the $\overline{INT}$ signal to stop the PCL5014.

- Reading ALM signal status
  Read bit 9 of status.
  0: $\overline{\text{ALM}}$ signal OFF
  1: $\overline{\text{ALM}}$ signal ON
- External input signal filter
  Set bit 8 of R6 at—
  0: Minimum pulsewidth is 64 cycles at the reference clock.
  1: External input filter OFF

5.4.6 Manual Pulser Input

For manual operation of a device, you may use a manual pulser such as a rotary encoder. The PCL504 can input signals from the pulser and output corresponding pulses from the $\overline{OUT}$ and DIR pins, thereby allowing you to simplify the external circuit and control the present position of axis. The manual pulser input is effective between the start of constant-speed operation at the FH pulse rate and the cessation by the immediate stop command in the preset mode 2 and between the start of constant-speed operation at the FH pulse rate and the completion of operation in the preset mode 4. Also, the microstep control is effective for the pulser input.

The PCL5014 receives plus and minus pulses or 90° phase difference signals from the pulser at PA and PB pins. You can select the input mode with bits 13 and 12 of R6. The 90° phase difference signals can be input through multiplication by 1, 2 or 4.

In the continuous mode 2, the moving direction of PCL5014 depends on the rotating direction of pulser. But in the preset mode 4, the moving direction of PCL5014 is as written in the operation mode buffer and has no concern with the rotating direction of pulser.

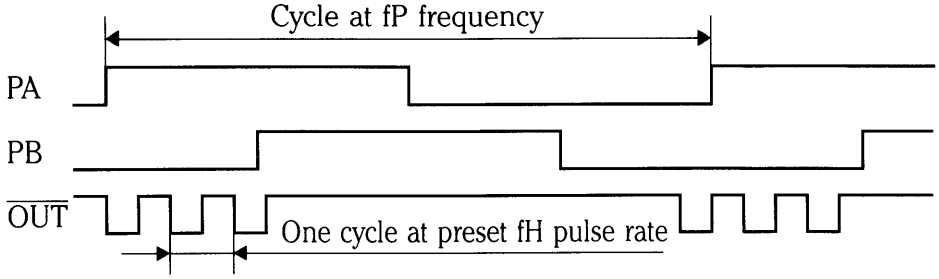
If the PCL5014 inputs 90° phase difference signals In the continuous mode 2, the moving direction is plus when the phase of the signal to the PA pin advances over that to the PB pin. In the case of two-pulse input, the PCL5014 moves in the plus direction at the edge of PA input changing from low to high.

The PCL5014 outputs the $\overline{INT}$ signal if levels of PA and PB signals change simultaneously or if the input frequency exceeds the range. A maximum input frequency of pulser signals is limited by the FH pulse rate. Relations between the FH pulse rate "fH" (pps) and the pulser input frequency "fP" (pps) should be as follows.

n = Unit number of output pulses

PA & PB Input Mode	Applicable Range
1 time multiplied 90° phase difference signal	fP < fH/(n +1)
2 times multiplied 90° phase difference signal	fP < fH/[(n +1) x 2)]
4 times multiplied 90° phase difference signal	fP < fH/[(n +1) x 4)]
2-pulse input	fP < fH/(n +1)

Example: If 1 time multiplied 90° phase difference signals are input with the unit number of output pulses set at 3 (set number = 2)



- Pulser input applicable operation modes
  Set bits 3 to 0 of the operation mode buffer at—
  0001: Continuous mode 2
  1100: Preset mode 4
- Select the moving direction in the preset mode 4 by setting bit 4 of the operation mode buffer at—
  0: Plus direction
  1: Minus direction
- Select the PA/PB input mode by setting bits 13 and 12 of R6 at—
  00: 90° phase difference signals in 1x mode
  01: 90° phase difference signals in 2x mode
  10: 90° phase difference signals in 4x mode
  11: Plus and minus pulses
- Interrupt status code for PA/PB input error
  The interrupt status code 12HEX indicates that the $\overline{\text{INT}}$ signal was initiated by simultaneous change of PA and PB input signals or the input frequency which exceeds the maximum level.

5.4.7 Up/Down Counter

The PCL5014 has a 28-bit binary up/down counter for managing the present position. In the preset mode 3, the number of pulses to move the axis is internally calculated referring to this counter. It counts output pulses or EA and EB input signals. You can select either with bit 27 of R6. If you select EA and EB signals, input plus and minus pulses or 90° phase difference signals to these pins. The up/down counter can count 90° phase difference signals multiplied by 1, 2 or 4. If you let the up/down counter count output pulses, it counts full-step positions even under the microstep control. If you let it count EA and EB signals and use the microstep control function, input pulse signals with a resolution of the full-step position. If EA and EB signals change simultaneously, an error result, thereby letting the PCL5014 output the $\overline{\text{INT}}$ signal.

With R6 you can select an up/down counter range, 0 to 268,435,455 or −134,217,728 to +134,217,727.

Selection of a range does not affect the operation of up/down counter but changes the following.

(1) Method of calculating the number of pulses (moving amount) in the preset mode 3 and zero return mode.
(2) Comparison method of comparator function
(3) Method of extending a code in reading the up/down counter, R10 and R11.

The up/down counter stops counting when it is suspended by setting or in the timer mode where output pulses are counted. Also, the up/down counter is reset by the following events.

(1) Writing the up/down counter reset command
(2) $\overline{CLR}$ input pin changes from high to low level.
(3) Completion of origin return (only with bit 6 of R7 set at 1)
(4) Writing 0 into the R9.

R8 allows you to let $\overline{CLR}$ signal initiate the $\overline{INT}$ signal. You can read the counter value directly through the direct port 1 without writing the read command. In reading 32 bits, high-place 4 bits are code-extended according to the counting range selected by bit 28 of R6.

- To select whether or not to operate the up/down counter, set bit 6 of the operation mode buffer at—
  0: Operates
  1: Does not operate
- To select the type of input signal to the up/down counter, set bit 27 of R6 at—
  0: Output pulses
  1: EA and EB input signals; EA/EB input error initiates the $\overline{INT}$ signal.
- To select the counting range, set bit 28 of R6 at—
  0: 0 to 268,435,455 ($FFFFFFF_{HEX}$)
  1: −134,217,728 (8000000_{HEX}) to +134,217,727 ($7FFFFFF_{HEX}$)
- To select the EA/EB input mode, set bits 10 and 10 of R6 at—
  00: 90° phase difference signals in 1x mode
  01: 90° phase difference signals in 2x mode
  10: 90° phase difference signals in 4x mode
  11: Plus and minus pulses
- Interrupt status code for EA/EB input error
  The interrupt status code 11_{HEX} indicates that the $\overline{INT}$ signal was initiated by simultaneous change of EA and EB signals, provided that the up/down counter input is output pulses.
- To let the completion of origin return reset the up/down counter, set bit 6 of R7 at 1.
- To let the $\overline{CLR}$ signal initiate the $\overline{INT}$ signal, set bit 7 of R8 at 1.
- Interrupt status code for $\overline{CLR}$ signal input
  The interrupt status code 10_{HEX} indicates that the $\overline{CLR}$ signal resets the up/down counter.
- To read the $\overline{CLR}$ pin status, read status bit 12—
  0: OFF
  1: ON

- To reset the up/down counter, write the up/down counter clear command 61HEX to the command buffer.

5.4.8 Comparator

The PCL5014 has two built-in 28-bit comparator circuits and can compare parameters of R10 and R11 with a counter value. You can select the counter to be subjected to comparison, the up/down counter or preset counter, by so setting bit 22 of R7. When a result of comparison meets with the comparator condition, the $\overline{\text{CMP}}$ signal becomes low level. Select one of 13 conditions by using R7.

Also, you can select the transaction the PCL5014 takes when the comparator condition is satisfied.

(1) No operation
(2) Immediately stops outputting pulses.
(3) Continues internal operation but does not output any pulse.
(4) Replaces the FH pulse rate and acceleration rate with those written in preregisters.

You can let the PCL 5014 output the $\overline{\text{INT}}$ signal when the comparator condition is satisfied. Note, however, that the $\overline{\text{INT}}$ signal is delayed until it completes the operation after the $\overline{\text{CMP}}$ signal is output if the condition (2) above is selected.

Precautions

- If you change the R3 preregister value (for the condition (4) above) with the automatic ramping-down point setting function activated by setting bit 1 of the control mode buffer at 0, the automatic setting function becomes impossible to perform to the specification.
- If you select the up/down counter as a counter to be compared with parameters of R10 and R11, the counting range selected by setting bit 28 of R6 at 0 effects comparison in positive number and that selectet by setting bit 28 at 1 effects comparison in signed number. If you select the preset counter, comparison is always made in positive number. Take care of set parameters of R10 and R11.
- If you use an undefined code such as 1111 for the comparator condition, a comparison result is always false.
- To select the counter for comparison, set bit 22 of R7 at—
  0: Up/down counter
  1: Preset counter

- To select a comparator condition, set bits 19 to 16 of R7 as follows:

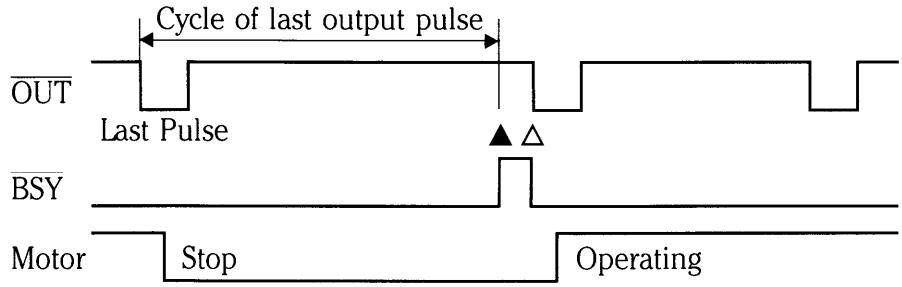
Bits of R7				Comparator Condition
19	18	17	16	
0	0	0	0	R10 > Counter value
0	0	0	1	R10 = Counter value
0	0	1	0	R10 < Counter value
0	1	0	0	R11 > Counter value
0	1	0	1	R11 = Counter value
0	1	1	0	R11 < Counter value
1	0	0	0	R10 > Counter value or R11 < Counter value
1	0	0	1	R10 < Counter value or R11 > Counter value
1	0	1	0	R10 = Counter value or R11 = Counter value
1	0	1	1	R10 > Counter value or R11 > Counter value
1	1	0	0	R10 < Counter value or R11 < Counter value
1	1	0	1	R10 < Counter value < R11
1	1	1	0	R10 > Counter value > R11

- To select the transaction the PCL5014 takes when the comparator condition is satisfied, set bits 21 and 20 of R7 at—
  00: No transaction
  01: Immediately stops outputting pulses.
  10: Continues internal operation but does not output any pulse.
  11: Replaces the FH pulse and acceleration rate with those written in preregisters.
- To check the $\overline{\text{CMP}}$ pin status
  Read the status bit 8.
  0: $\overline{\text{CMP}}$ pin OFF
  1: $\overline{\text{CMP}}$ pin ON
- To output the $\overline{\text{INT}}$ signal when the comparator condition is satisfied
  Set bit 13 of R8 at 1.
- To check the interrupt factor when the comparator condition is satisfied
  Read the interrupt status. If the interrupt status code at the $\overline{\text{INT}}$ signal output is 16HEX, it indicates that the comparison result changes from false to true.

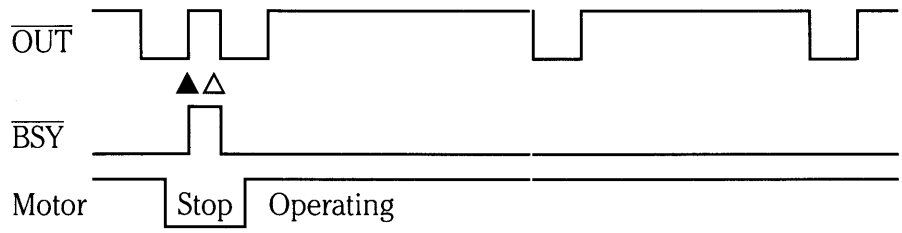
5.4.9 Controlling Time Width of Last Pulse Cycle

You can shorten the time width of the last pulse cycle to make the stop timing quicker. If the output pulse rate is lower than 1/8192 of the reference clock (2.4 Kpps with a reference clock of 19.6608MHz), the output pulsewidth is fixed to a time length of 4096 cycles at the reference clock (approximately 200μs with a reference clock of 19.6608MHz). If the output pulse rate is higher than 1/8192 of the reference clock, pulses are output at a constant duty cycle (approximately 50%). Note, however, that if R4 is set at 1, the pulsewidth is fixed to two cycles at the reference clock. By setting bit 7 of the operation mode buffer at 1, you can shorten the time between the last pulse output and the completion of operation.

(1) With bit 7 set at 0 (completion in one cycle of the last pulse)



(2) With bit 7 set at 1 (completion upon pulse off)



▲: Timing to stop the motor from operating

△: Timing to start the next operation

- To select the operation completion timing

  Set bit 7 of the operation mode buffer at—

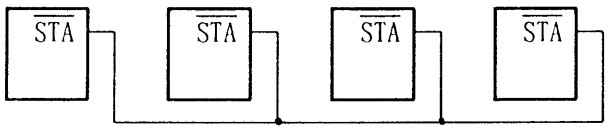
  0: Upon completion of the last pulse cycle

  1: When the last pulse output is OFF

5.4.10 Simultaneous Start

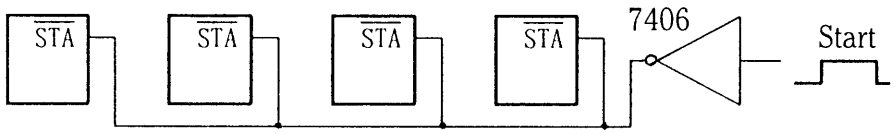
If you use multiple units of PCL3013, you can connect their $\overline{\text{STA}}$ pins together to start multiple motors simultaneously. In addition to the internal software signal, you can write an external hardware signal to start them simultaneously by driving the $\overline{\text{STA}}$ signal line with an output of open collector (74LS06 or the like). Also, under such the connection, you can start each motor individually.

(1) Connection for Simultaneous Start with Internal Signal



- Write operation parameters and the start retention command in each unit of PCL5014. Then write the simultaneous start signal in any of the units. The units in which the start retention command has been written will start generating pulses simultaneously.
- If you write an ordinary start command after writing operation parameters, only the concerned PCL5015 starts generating pulses.
- The simultaneous start command is effective for all $\overline{\text{STA}}$ pins connected.

(2) Connection for Simultaneous Start through External Circuit



The $\overline{\text{STA}}$ signal is output from the open collector. Use a one-shot signal, of which the pulsewidth should be 8 cycles or over at the reference clock.

Write operation parameters and the start retention command in each unit of PCL5014. Then an input of external start signal will start all units in which the start retention command has been written. The internal simultaneous start command too is effective under this connection.

NOTE: If you write the start retention command with the $\overline{\text{STA}}$ pin at low level, all units of PCL5014 start generating pulses immediately. To cancel the start retention status, write the immediate stop command or emergency stop command.

- To select the $\overline{\text{STA}}$ signal trigger mode

  Set bit 31 of R6 at—

  0: Level trigger

  1: Edge trigger

- To check the $\overline{\text{STA}}$ pin status

  Read bit 6 of R13.

  0: $\overline{\text{STA}}$ pin OFF

  1: $\overline{\text{STA}}$ pin ON

- To check the start retention status

  Read bit 6 of R14.

  1: $\overline{\text{STA}}$ signal is waited for.

  Or read status bits 2 to 0.

  010: $\overline{\text{STA}}$ signal is waited for.

- To simultaneously start multiple units of PCL5014
  Write the simultaneous start command 30HEX to the command buffer. One-shot pulse with a width of 512 cycles at the reference clock will be output from the $\overline{STA}$ pin.

5.4.11 Simultaneous Stop

If you use multiple units of PCL5014, connect $\overline{STP}$ pins of all units. Then you can stop all units simultaneously upon abnormal stop of any unit. Also, you can let the $\overline{STP}$ signal initiate the $\overline{INT}$ signal output.

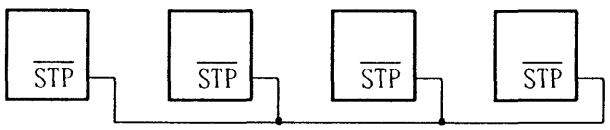
The control mode buffer allows you to select the simultaneous stop signal input function and the simultaneous stop signal output function. By setting these functions, you can place the system in a condition similar to the condition where $\overline{STP}$ pins are not connected or let the PLC5014 output the $\overline{STP}$ signal at an abnormal stop.

In addition, you can stop all units simultaneously with an external hardware signal by driving the $\overline{STP}$ signal line through an output of open collector (74LS06 or the like).

Abnormal stop here means any of the following events.

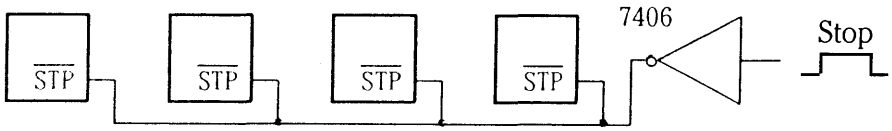
(1) The $\overline{+EL}$ or $\overline{-EL}$ signal stops the PCL5014 from generating pulses in other than the origin search mode.
(2) The $\overline{+SD}$ or $\overline{-SD}$ signal initiates deceleration then stops the PCL5014 from generating pulses in other than the origin search mode (with bit 29 of R6 set at 1).
(3) The $\overline{ALM}$ signal stops the PCL5014 from generating pulses.
(4) Detection of an out-of-step status stops the PCL5014 from generating pulses.
(5) A comparator condition is satisfied, thereby stopping the PCL5014 from generating pulses.
(6) The simultaneous stop command is written.

(1) Connection for Simultaneous Stop with Internal Software Signal



Set bits 5 and 6 of the control mode buffer at 1 and 0, respectively, with all units of PCL5014 so that the simultaneous stop signal input function and the simultaneous stop signal output function are valid. An abnormal stop of any unit will stop all the units of which the simultaneous stop signal input function is made valid.

(2) Connection for Simultaneous Stop through External Circuit



The $\overline{STP}$ signal is controlled by the open collector output. Use a one-shot signal, of which the pulsewidth should be eight cycles or over at the reference clock. The PCL5014 stops generating pulses when the $\overline{STP}$ pin changes from high to low level.

Set bit 5 of the control mode buffer at 1 to effect the simultaneous stop function of the concerned units of PCL5014.
Under this configuration, either external stop signal or internal stop signal stops all concerned units of PCL501.

NOTE: If the $\overline{STP}$ pin is at low level, writing the start signal does not start the PCL5014 of which the simultaneous stop function is turned on.

- To select the simultaneous stop signal input function
  Set bit 5 of the control mode buffer at—
  0: OFF (invalid)
  1: ON (valid)T
- To select the simultaneous stop signal output function
  Set bit 6 of the control mode buffer at—
  0: OFF (invalid)
  1: ON (valid)
- To output $\overline{INT}$ signal when the $\overline{STP}$ signal stops the PCL5014
  Set bit 15 of R8 at—
  0: None
  1: Yes
- To check the interrupt factor
  Read the interrupt status. If the interrupt status code is 06_{HEX}, it indicates that the $\overline{STP}$ signal stops the PCL5014.
- To check the $\overline{STP}$ pin status
  Read bit 7 of R13.
  0: $\overline{STP}$ pin OFF
  1; $\overline{STP}$ pin ON
- Simultaneous stop command 28_{HEX}
  Write it to the command buffer. The $\overline{STP}$ pin will output a one-shot pulse with a width of 12 cycles at the reference clock.

5.4.12 Dummy Operation

You can let the PCL5014 perform all activities except for pulse generation. This allows you to check the PCL5014 without moving the machine.

In the dummy operation, $\overline{OUT}$ and DIR pins do not output any pulse except in the common pulse mode where the PCL5014 outputs a direction signal if it is available at the DIR pin.

The up/down counter counts "output pulses" irrespective of R6 setting.

In the origin return mode, origin search mode and origin escape mode, the PCL5014 completes the dummy operation without outputting any pulse.

The PCL5014 continues the dummy operation if $\overline{\pm EL}$, $\overline{\pm SD}$ or $\overline{ALM}$ signal is turned on.

The $\overline{INT}$ signal does not delay the timing of the completion of operation.

- To effect the dummy operation
  Set bit 7 of R7 at—
  0: OFF
  1: ON

5.4.13 General-Purpose I/O Ports with Interrupt Signal Input Function

The PCL5014 has three general-purpose I/O ports, AP0, AP1 and AP2. If you connect the CPU with the CPU interface as an 8-bit bus, you can use pins D8 to D15 as general-purpose ports BP0 to BP7. Though under the default condition these pins are defined as input ports, you can individually re-define them as output ports by setting bits 16–26 of R6.

You can control the output of BP0 to BP7 by writing data in the general-purpose I/O buffer or with a command and check the status by reading the general-purpose I/O buffer irrespective of input or output. Similarly, you can control the output of AP0 to AP2 with a command and read the status irrespective of input or output. The initial level of the output latch circuit for all these general-purpose ports AP0 to AP2 and BP0 to BP7 is 0 (low level). You can write data in the output latch circuit if you use the pin as input. If you change the definition from input to output or vice versa, the latch status does not change. In addition, you can use general-purpose ports AP0, AP1 and AP2 as interrupt signal input ports by setting bits 4, 5 and 6 of R8. Irrespective of definition of input or output, the $\overline{INT}$ signal is output when any of these pins changes from high to low level. Since these pins are at CMOS level, connect a pull-up resistor of 1kΩ to 100kΩ to any of the pins which are not used.

- To define general-purpose I/O ports as input or output
  Set bits 26, 25 and 24 (for AP2, AP1 and AP0, respectively) and bts 23 to 16 (for BP7 to BP0) at—
  0: Defined as input port
  1: Defined as output port
  Setting of BP7 to BP0 is effective with B/$\overline{W}$ pin at high level.
  Under the default condition, all pins are defined as input ports since R6 = 0.

- To control the output of ports AP2, AP1 and AP0, write the following commands to the command buffer:
  - A4HEX: Places the AP2 port at low level.
  - 49HEX: Places the AP1 port at low level.
  - 48HEX: Places the AP0 port at low level.
  - 5AHEX: Places the AP2 port at high level.
  - 59HEX: Places the AP1 port at high level.
  - 58HEX: Places the AP0 port at high level.
- To control the output of ports BP7 to BP0, set bits 7 to 0 (for BP7 to BP0, respectively) at—
  - 0: High level
  - 1: Low level

  Or, write the following commands to the command buffer:
  - 47HEX: Places the BP7 port at low level.
  - 46HEX: Places the BP6 port at low level.
  - 45HEX: Places the BP5 port at low level.
  - 44HEX: Places the BP4 port at low level.
  - 43HEX: Places the BP3 port at low level.
  - 42HEX: Places the BP2 port at low level.
  - 41HEX: Places the BP1 port at low level.
  - 40HEX: Places the BP0 port at low level.
  - 57HEX:Places the BP7 port at high level.
  - 56HEX: Places the BP6 port at high level.
  - 55HEX: Places the BP5 port at high level.
  - 54HEX: Places the BP4 port at high level.
  - 53HEX: Places the BP3 port at high level.
  - 52HEX: Places the BP2 port at high level.
  - 51HEX: Places the BP1 port at high level.
  - 50HEX: Places the BP0 port at high level.
- To check the status of ports AP2, AP1 and AP0, read status bits 15, 14 and 13, respectively.
  - 0: Low level
  - 1: High level
- To check the status of ports BP7 to BP0, read status bits 7 to 0, respectively.
  - 0: Low level
  - 1: High level
- To output the $\overline{INT}$ signal with ports AP2, AP1 and AP0 defined as input ports, set bits 6, 5 and 4 (for AP2, AP1 and AP0, respectively) at—
  - 1: The $\overline{INT}$ signal is output when ports AP2, AP1 and AP0 change from high to low level.

- To check the factor initiating the $\overline{INT}$ signal, read the interrupt status code:
  0F$_{HEX}$: The AP2 port changes from high to low level.
  0E$_{HEX}$: The AP1 port changes from high to low level.
  0D$_{HEX}$: The AP0 port changes from high to low level.
- To select CPU interface bits, place the B/$\overline{W}$ pin (pin 15) at high level to select 8 bits or at low level to select 16 bits.

5.4.14 External Input Signals from Mechanical System

The PCL5014 can input the following five signals as position detecting signals from the mechanical system.

(1) $\overline{+EL}$ and $\overline{-EL}$ Signals

In other than the origin search mode, the EL signal in the moving direction ($\overline{+EL}$ signal in moving in plus direction) immediately stops PCL5014 from generating pulses while the $\overline{INT}$ signal is output and thereafter keeps it stopped if the signal recovers the OFF status. If you write the start command with this signal ON, the PCL5014 does not start generating pulses for that direction while outputting the $\overline{INT}$ signal. In the origin search mode, the EL signal in the moving direction reverses the moving direction and does not accompany the $\overline{INT}$ signal.

$\overline{+EL}$ and $\overline{-EL}$ signals may be pulse signals, of which the shortest width is usually a time length of 64 cycles at the reference clock (approximately 3μs with a reference clock of 19.6608MHz). However, you can make it a time length of 2 cycles at the reference clock (approximately 0.1μs with a reference clock of 19.6608MHz) by setting bit 8 of R6 at 1 to turn the input filter off. The microstep control, if used, delays the stop timing until all pulses in the unit number are output. However you can stop PCL5014 before outputting all pulses in the unit number by setting bit 23 of R7 at 1.

You can check ON/OFF conditions of these signals by reading the status code. Also, note that these signals are neglected in the timer mode and dummy operation (with bit 7 of R7 set at 1) but the status can be monitored. For safety, you cannot change the input logic.

- Interrupt status Code
  08$_{HEX}$: $\overline{+EL}$ signal initiated the $\overline{INT}$ signal.
  07$_{HEX}$: $\overline{-EL}$ signal initiated the $\overline{INT}$ signal.
- To check $\overline{\pm EL}$ signal status, read status bits 4 and 3.
  0: OFF
  1: ON
- To select the external signal input filter mode, set bit 6 of R9 at—
  0: Minimum pulsewidth 64 cycles at the reference clock
  1: External signal input filter OFF

(2) $\overline{+SD}$ and $\overline{-SD}$ Signals

By setting bit 29 of R6, you select whether these signals effect deceleration only or stop after deceleration. By setting bit 5 of the operation mode buffer, you can select whether these signals are made valid or invalid. You can also latch OFF-ON change by setting R6. In such a case the next start or a latch input setting cancels the latched condition. The default input logic is negative but you can change it to the positive logic by setting bit 4 of R6. You can check ON/OFF conditions of these signals by reading the status code. An input filter is provided as for ±EL signals.

- Deceleration only

  When the ramping-down signal in the moving direction ($\overline{+SD}$ or $\overline{-SD}$) is turned on during varied-speed operation, the PCL5014 decelerates the pulse output to the FL rate. When the signal is turned off during or after deceleration, the PCL5014 accelerates the pulse output to the FH rate. If the signal is on at the start, the PCL5014 does not accelerate the pulse output to the FH rate but keeps outputting pulses at the FL rate. $\overline{SD}$ signals are invalid in the constant-speed mode.

- Stop after deceleration

  When the ramping-down signal is turned on during varied-speed operation, the PCL5014 decelerates the pulse output to the FL rate then stops generating pulses. If the signal is turned off during deceleration, the PCL5014 accelerates the pulse output but if it is turned off after deceleration completed, the PCL5014 keeps the stop condition. If the signal is turned on during constant-speed operation at the FL pulse rate, the PCL5014 immediately stops generating pulses but if the signal is turned on during constant-speed operation at the FH rate, $\overline{SD}$ signals are neglected.

- To make the $\overline{\pm SD}$ signal control valie or invalid, set bit 5 of the operation mode buffer at—
  0: Valid
  1: Invalid

- To select deceleration only or stop after deceleration, set bit 29 of R6 at—
  0: Deceleration only
  1: Stop after deceleration

- To select the input logic of $\overline{\pm SD}$ signal, set bit 4 of R6 at—
  0: Negative
  1: Positive

- To select the trigger mode of $\overline{\pm SD}$ signal (and $\overline{ORG}$ signal), set bit 30 of R6 at—
  0: Level trigger
  1: Latch trigger

The latched condition is cancelled by the next start or by setting to level trigger.

- To check the interrupt factor, read the interrupt status code:
  OAHEX: $\overline{+SD}$ initiated the $\overline{INT}$ signal.
  09HEX: $\overline{-SD}$ initiated the $\overline{INT}$ signal.
- To check the $\overline{\pm SD}$ signal status, read status bits 6 and 5 (for $\overline{-SD}$ and $\overline{+SD}$, respectively).
  0: OFF
  1: ON (the latched condition is read in the case of latch input)
- To select the external signal input filter mode, set bit 8 of R6 at—
  0: Minimum pulsewidth 64 cycles at the reference clock
  1: External input signal filter OFF
- To output the $\overline{INT}$ signal at the start of deceleration, set bit 3 of R8 at:
  1: $\overline{INT}$ signal output
- To check the interrupt factor, read the interrupt status code:
  15HEX: The ramping-down signal initiated the $\overline{INT}$ signal.

(3) $\overline{ORG}$ Signal

Use this signal for origin return. Motion control using this signal is available in the origin return modes 1 and 2, origin search mode and origin escape mode. The OFF-ON change can be latched by setting R6. In such a case the latched condition can be cancelled by the next start or by cancelling the latch input setting. The default input logic is negative but you can change it to the positive logic. If you need to stop the PCL5014 after counting the $\overline{EZ}$ signal, you should keep placing the $\overline{ORG}$ signal in the ON status until the PCL5014 stops. Or you should select the latch input. If you stop the PCL5014 with the $\overline{ORG}$ signal only, it may be a pulse signal, of which the shortest width is usually a time length of 64 cycles at the reference clock (approximately 3μs with a reference clock of 19.6608MHz). However, you can make the pulsewidth a time length of two cycles at the reference clock (approximately 0.1μ with a reference clock of 19.6608MHz) by turning the external input filter off. You can check the ON/OFF condition of the signal by reading the status code.

- To select the input logic of $\overline{ORG}$ signal, set bit 5 of R6 at—
  0: Negative logic
  1: Positive logic
- To select the trigger mode of $\overline{ORG}$ signal (and $\overline{\pm SD}$ signal), set bit 30 of R6 at—
  0: Level trigger
  1: Latch trigger

- To check the interrupt factor, read the interrupt status code:
  03HEX: Completion of origin return or search initiated the $\overline{INT}$ signal.
- To check the $\overline{ORG}$ signal status, read the status bit 7.
  0: OFF
  1: ON (latched condition is read in the case of latch input)
- To select the condition at the completion of origin return, set bits 5 and 4 of R7 at—
  00: Stop upon $\overline{ORG}$ signal turning ON
  10: $\overline{ORG}$ signal initiates deceleration and $\overline{EZ}$ counting then stops the PCL5014 from generating pulses.
  01: $\overline{ORG}$ signal initiates $\overline{EL}$ counting then stops the PCL5014 from generating pulses.
  11: Setting prohibited
  (The $\overline{ORG}$ signal must be off at the completion of origin escape.)
- To select the $\overline{EZ}$ counts at the completion of origin return, set bits 3 to 0 at—
  (counts − 1) in a range of 0 to 15.
- To check the EZ counter value, read bits 19 to 16 of R12.
- To select the input logic of $\overline{EZ}$ signal, set bit 7 of R6 at—
  0: Negative logic
  1: Positive logic
- To check the $\overline{EZ}$ signal status, read bit 7 of R14.
  0: OFF
  1: ON
- To select the external signal input filter mode, set bit 8 of R6 at—
  0: Minimum pulsewidth 64 cycles at the reference clock
  1: External signal input mode OFF

5.4.15 Pulse Output Mode

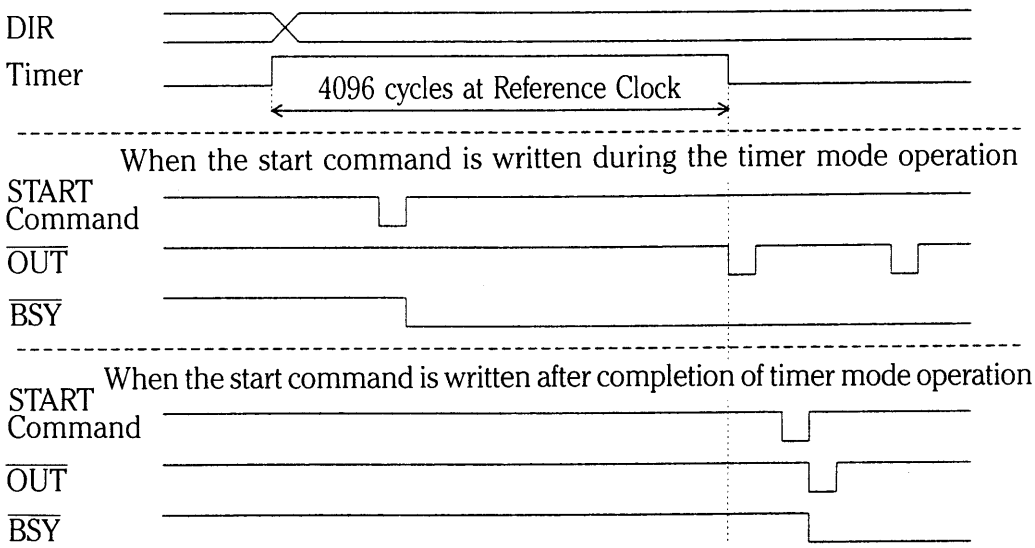
You can select the common pulse mode or the 2-pulse mode by setting of R6 and the output logic of $\overline{OUT}$ and DIR pins.

If you select the common pulse mode, the $\overline{OUT}$ pin outputs operating pulses in no relation with the moving direction and the DIR pin outputs a level signal for direction judgment. In the negative output logic, the high level direction judgment signal indicates plus direction and the low level signal indicates minus direction.

If you select the 2-pulse mode, the $\overline{OUT}$ pin outputs operating pulses in plus direction and the DIR pin outputs operating pulses in minus direction.

In the common pulse mode the driver requires a time from receiving the direction signal to accepting pulses. By effecting the direction switching timer, you can secure a time length of 4096 cycles at the reference clock (approximately 200μs with a reference clock of 19.6608MHz) for the time from a change of the direction signal to the output of pulses.

Start Timing Delayed due to Direction Change in Timer Mode Operation



- To select the pulse output mode, set bit 2 of R6 at—
  0: Common pulse mode
  1: 2-pulse mode
- To select the $\overline{OUT}$ signal output logic, set bit 0 of R6 at—
  0: Negative logic
  1: Positive logic
- To select the DIR signal output logic, set bit 1 of R6 at—
  0: Negative logic
  1: Positive logic
- To select the direction switching timer operation, set bit 11 of R7 at—
  0: No delay of operation at direction switchover
  1: Start of operation at direction switchover is delayed by 4096 cycles at the reference clock

5.4.16 Interrupt Signal Output

The PCL5014 can output the $\overline{INT}$ signal to the CPU according to 22 types of factors. These interrupt factors are coded and can be read as interrupt status. If two or more factors are generated simultaneously, they are read in the order from the larger code number and not in the order of generation. Reading all factors returns the $\overline{INT}$ signal to the high level.

If you use multiple units of PCL5014, you can connect their $\overline{INT}$ pins together in the wired OR mode. Note that such wired OR connection requires an external pull-up resistor of 5kΩ to 10kΩ.

Interrupt Signal Generating Factors

Code	Factor	Setting to Effect Interrupt
00HEX	$\overline{\text{INT}}$ output OFF	
01HEX	Deceleration-stop (0AHEX) command	Bit 0 of R8 = 1
02HEX	In-positioning	Bit 1 of R8 = 1
03HEX	Origin return (or origin search) completed	Bit 2 of R8 = 1
04HEX	Origin escape completed	Bit 2 of R8 = 1
05HEX	Immediate stop command (09HEX)	Bit 0 of R8 = 1
06HEX	$\overline{\text{STP}}$ signal ON	Bit 5 of operation mode buffer = 1
07HEX	$\overline{-\text{EL}}$ signal ON to stop	
08HEX	$\overline{+\text{EL}}$ signal ON to stop	
09HEX	$\overline{-\text{SD}}$ signal ON to deceleration-stop	Bit 29 of R6 = 1
0AHEX	$\overline{+\text{SD}}$ signal ON to deceleration stop	Bit 29 of R6 = 1
0BHEX	$\overline{\text{ALM}}$ signal ON to stop	
0CHEX	Detection of out-of-step status to stop	Bits 12 to 8 of R8 $\neq$ 00000
0DHEX	AP0 pin changes from high to low level	Bit 4 of R8 = 1
0EHEX	AP1 pin changes from high to low level	Bit 5 of R8 = 1
0FHEX	AP2 pin changes from high to low level	Bit 6 of R8 = 1
10HEX	$\overline{\text{CLR}}$ singal resets the up/down counter.	Bit 7 of R8 = 1
11HEX	Error in receiving EA and EB signals	Bit 27 of R6 = 1
12HEX	Error in receiving PA and PB signals	In continuous mode 2 or preset mode 4
13HEX	Error in receiving ERA and ERB signals	Bits 12 to 8 of R8 $\neq$ 00000
14HEX	Start of next operation*	Bit 14 of R8 = 1
15HEX	Start of deceleration	Bit 3 of R8 = 1
16HEX	Comparate condition changes from false to true.	Bit 13 of R8 = 1

5.5 Command Buffer

You can write the following commands in the command buffer. Do not write other than those described below.

5.5.1 Start Commands

(1) 10HEX for Constant-Speed Operation at FL Pulse Rate
Write this command when the PCL5014 stops generating pulses. It will generate pulses at the FL pulse rate (R1 x R4). Write the command when the PCL5014 is generating pulses. The command will be the start command for the next operation.

(2) 11HEX for Constant-Speed Operation at FH Pulse Rate
Write this command when the PCL5014 stops generating pulses. It will generates pulses at the FH pulse rate (R2 x R4). Write the command when the PCL5014 is generating pulses, the command will be the start command for the next operation.

(3) 13HEX for Varied-Speed Operation
Write this comand when the PCL5014 stops generating pulses. It will start generating pulses at the FL pulse rate then accelerate the pulse output to the FH pulse rate. Write the command when the PCL5014 is generating pulses. The command will be the start command for the next operation.

(4) 14HEX to Output Remaining Pulses for Suspended Constant-Speed Operation at FL Pulse Rate
Write this command after stopping the PCL5014 on the way of preset mode operation. The PCL5014 will output remaining pulses at the FL pulse rate. The command written during operation in progress has no function.

(5) 15HEX to Output Remaining Pulses for Suspended Constant-Speed Operation at FH Pulse Rate
Write this command after stopping the PCL5014 on the way of preset mode operation. The PCL5014 will output remaining pulses at the FH pulse rate. The command written during operation in progress has no function.

(6) 17HEX to Output Remaining Pulses for Suspended Varied-Speed Operation
Write this command after stopping the PCL5014 on the way of preset mode operation. The PCL5014 will start generating pulses at the FL pulse rate then accelerate the pulse output to the FH pulse rate to output remaining pulses. The command written during operation in progress has no function.

(7) 30HEX for Simultaneous Start

Writing this command lets the $\overline{STA}$ pin output the simultaneous start signal of one-shot pulse. If $\overline{STA}$ pins of plural units of PCL5014 are connected together, the units which are placed in the start retention status will start simultaneously.

5.5.2 Pulse Rate Switchover Commands

(1) 00HEX for Instantaneous Switchover to FL Pulse Rate

Write this command during operation in progress. The pulse rate will instantaneously be switched to the FL pulse rate. Writing the command during cessation has no function.

(2) 01HEX for Instantaneous Switchover to FH Pulse Rate

Write this command during operation in progress. The pulse rate will instantaneously be switched to the FH pulse rate. Writing the command during cessation has no function.

(3) 02HEX for Ramping-down to FL Pulse Rate

Write this command during operation in progress. The pulse rate ramps down to the FL pulse rate. Writing the command during cessation has no function.

(4) 03HEX for Ramping-up to FH Pulse Rate

Write this command during operation in progress. The pulse rate ramps up to the FH pulse rate. Writing the command during cessation has no function.

5.5.3 Stop Commands

(1) 09HEX for Immediate Stop

Write this command during operation in progress. The PCL5014 will immediately stop generating pulses while cancelling the start command for the next operation if entered. Writing command during cessation has no function.

(2) 0AHEX for Deceleration-Stop

Write this command during constant-speed operation at the FL pulse rate. The PCL5014 will immediately stop generating pulses. Write the command during constant-speed operation at the FH pulse rate or during varied-speed operation. The PCL5014 will decelerate the pulse output to the FL pulse rate then stop generating pulses while cancelling the start command for the next operation if entered. Writing the command during cessation has no function.

(3) 28HEX for Simultaneous Stop

Writing this command lets the $\overline{STP}$ pin output the simultaneous stop signal of one-shot pulse. If $\overline{STP}$ pins of plural units of PCL5014 are connected together, the command immediately stops all units of PCL5014

for which the simultaneous stop funtion is turned on by setting bit 5 of the control mode buffer at 1.

5.5.4 Start Retention Commands

(1) 20HEX for Retention of Constant-Speed Operation at FL Pulse Rate
Writing this command during cessation will cause the PCL5014 to be placed in standby condition for $\overline{\text{STA}}$ signal. When it receives the $\overline{\text{STA}}$ signal, the PCL5014 starts the constant-speed operation at the FL pulse rate. The command written during operation in progress is the start command for the next operation.

(2) 21HEX for Retention of Constant-Speed Operation at FH Pulse Rate
Write this command during cessation. The PCL5014 will be placed in the standby condition for the $\overline{\text{STA}}$ signal. When it receives the $\overline{\text{STA}}$ signal, the PCL5014 starts the constant-speed operation at the FH pulse rate. The command written during operation in progress is the start command for the next operation.

(3) 23HEX for Retention of Varied-Speed Operation
Write this command during cessation. The PCL5014 will be placed in the standby condition for the $\overline{\text{STA}}$ signal. When it receives the $\overline{\text{STA}}$ signal, the PCL5014 starts the varied-speed operation. The command written during operation in progress is the start command for the next operation.

(4) 24HEX for Retention of Suspended Constant-Speed Operation at FL Pulse Rate
Write this command during cessation. The PCL5014 will be placed in the standby condition for the $\overline{\text{STA}}$ signal. When it receives the $\overline{\text{STA}}$ signal, the PCL5014 outputs remaining pulses at the FL pulse rate. The command written during operation in progress has no function.

(5) 25HEX for Retention of Suspended Constant-Speed Operation at FH Pulse Rate
Write this command during cessation. The PCL5014 will be placed in the standby condition for the $\overline{\text{STA}}$ signal. When it receives the $\overline{\text{STA}}$ signal, the PCL5014 outputs remaining pulses at the FH pulse rate. The command written during operation in progress has no function.

(6) 27HEX for Retention of Suspended Varied-Speed Operation
Write this command during cessation. The PCL5014 will be placed in the standby condition for the $\overline{\text{STA}}$ signal. When it receives the $\overline{\text{STA}}$ signal, the PCL5014 starts outputting pulses at the FL pulse rate then accelerate the pulse output to the FH pulse rate to output all remaining pulses for the varied-speed operation. The command written during operation in progress has no function.

5.5.5 General-Purpose I/O Bit Setting Commands

If the general-purpose I/O pins are defined as output, use the following commands to put them at low or high level:

40HEX	Places general-purpose output pin BP0 at low level.
41HEX	Places general-purpose output pin BP1 at low level.
42HEX	Places general-purpose output pin BP2 at low level.
43HEX	Places general-purpose output pin BP3 at low level.
44HEX	Places general-purpose output pin BP4 at low level.
45HEX	Places general-purpose output pin BP5 at low level.
46HEX	Places general-purpose output pin BP6 at low level.
47HEX	Places general-purpose output pin BP7 at low level.
48HEX	Places general-purpose output pin AP0 at low level.
49HEX	Places general-purpose output pin AP1 at low level.
4AHEX	Places general-purpose output pin AP2 at low level.
50HEX	Places general-purpose output pin BP0 at high level.
51HEX	Places general-purpose output pin BP1 at high level.
52HEX	Places general-purpose output pin BP2 at high level.
53HEX	Places general-purpose output pin BP3 at high level.
54HEX	Places general-purpose output pin BP4 at high level.
55HEX	Places general-purpose output pin BP5 at high level.
56HEX	Places general-purpose output pin BP6 at high level.
57HEX	Places general-purpose output pin BP7 at high level.
58HEX	Places general-purpose output pin AP0 at high level.
59HEX	Places general-purpose output pin AP1 at high level.
5AHEX	Places general-purpose output pin AP2 at high level.

5.5.6 Control Commands

(1) 60HEX for Software Reset

This command resets the PCL5014 (the same effect as the $\overline{RST}$ pin at low level). After writing this command, do not try to access to the PCL5014 for a time length of 16 cycles at the reference clock (approximately 0.8μs with a reference clock of 19.6608MHz).

(2) 61HEX to Reset Up/Down Counter

This command resets the up/down counter R9 to 0.

(3) 62HEX to Reset Deviation Counter for Out-of-Step Detection

This command resets the deviation counter for out-of-step detection to 0.

(4) 63HEX for Emergency Stop

This command lets the PCL5014 output the $\overline{ERC}$ signal in one shot. Writing this command during operation in progress stops the PCL5014

immediately from generating pulses. The command neglects the unit number of output pulses under the microstep control and may shorten the width of the last output pulse.

(5) 66HEX to Put Preregisters in Settled Status
This command puts preregisters in settled status.

(6) 67HEX to Put Preregisters in Unsettled Status
Writing the start command during operation in progress lets the PCL5014 judge that the preparation for the next operation is complete and automatically start the next operation upon completion of the present operation. This command allows you to cancel such the status so as not to start the next operation.

5.5.7 Register Read Commands

Register read commands copy register contents on the input/output buffer then let the CPU read them from the input/output buffer.

Command	Reading Parameter
80HEX	Number of output pulses entered in R0 register
81HEX	FL pulse rate entered in R1 register
82HEX	FH pulse rate entered in F2 register
83HEX	Accel/decel rate entered in R3 register
84HEX	Multiplication factor entered in R4 register
85HEX	Ramping-down point entered in R5 register
86HEX	Environmental condition 1 set by R6 register
87HEX	Environmental condition 2 set by R7 register
88HEX	Environmental condition 3 set by R8 register
89HEX	Up/down counter value saved in R9 register
8AHEX	Comparator 1 data saved in R10 register
8BHEX	Comparator 2 data saved in R11 register
8CHEX	Counter data saved in R12 register
8DHEX	Command status 1 saved in R13 register
8EHEX	Command status 2 saved in R14 register
90HEX	Output pulses for next operation entered in R0 preregister
91HEX	FL pulse rate for next operation entered in R1 preregister
92HEX	FH pulse rate for next operation entered in R2 preregister
93HEX	Accel/decel rate for next operation entered in R3 preregister
94HEX	Multiplication factor for next operation entered in R4 preregister
95HEX	Preset counter value
96HEX	Ramping-down point counter value
97HEX	Ramping-down point entered in R5 preregister
98HEX	Deceleration rate for next operation entered in R15 preregister
99HEX	S-curve related parameter for next operation entered in R16 preregister
9AHEX	Deceleration rate entered in R15 register
9BHEX	S-curve related parameter entered in R16 register

5.5.8 Register Write Commands

Register write commands copy the contents of the input/output buffer onto registers. Let the CPU write data in the input/output buffer in advance.

Parameters entered in preregisters are copied into the respective registers at the time of starting the next operation.

Command	Writing Parameter
C0HEX	Number of output pulses into R0 preregister
C1HEX	FL pulse rate into R1 preregister
C2HEX	FH pulse rate into F2 preregister
C3HEX	Acceleration rate into R3 preregister
C4HEX	Multiplication factor into R4 preregister
C5HEX	Ramping-down point into R5 preregister
C6HEX	Environmental condition 1 into R6 register
C7HEX	Environmental condition 2 into R7 register
C8HEX	Environmental condition 3 into R8 register
C9HEX	Up/down counter value into R9 register
CAHEX	Comparator 1 data into R10 register
CBHEX	Comparator 2 data into R11 register
D1HEX	Change of FL pulse rate under operation into R1 register
D2HEX	Change of FH pulse rate under operation into R2 register
D3HEX	Change of acceleration rate under operation into R3 register
D7HEX	Change of ramping-down point under operation into R5 register
D8HEX	Deceleration rate into R15 preregister
D9HEX	S-curve related parameter into R16 preregister
DAHEX	Change of deceleration rate under operation into R15 register
DBHEX	Change of S-curve related parameter under operation into R16 register

5.6 Registers

5.6.1 R0—Output Pulse Register, 28-bit

This register sets a target position in the number of output pulses. In the origin return mode 2 and preset mode 1, it retains the number of output pulses with no sign (0 to 268,435,455). In the preset mode 2, it retains the number of output pulses with a sign (−134,217,728 to +134,217,727). In the preset mode 3, the presence or absence of a sign depends on a selected counting range of up/down counter. Write the parameter into the preregister. If the parameter is the same as previous, you need not write it anew. When the parameter is read as 32-bit data, high-place four bits are all 0.

The parameter written in the preregister is copied from the preregister R0 to the register R0 at the start then converted into a moving amount to be loaded in the preset counter. After starting, the counter counts down at every output of pulses in the unit number. However, it does not count down if bit 0 of the control mode buffer is set at 1. Also, under the microstep control, the number of output pulses is (preset counter value x unit number of output pulses). Set the unit number with R7. Refer to "5.4.2 Microstop Control" for details.

- To effect the preset counter, set bit 0 of the control mode buffer at—
  0: Normal counting
  1: No counting
- To select the counting range of up/down counter, set bit 28 of R6 at—
  0: 0 to 268,435,455 ($FFFFFFF_{HEX}$)
  1: −134,217,728 (8000000_{HEX}) to +134,217,727 ($7FFFFFF_{HEX}$)
- To select the unit number of output pulses for microstep control, set bits 31 to 24 of R7 at—
  (resolution of microstep − 1)
  The setting range is 0 to 255.

5.6.2 R1—FL Pulse Rate Register, 15-bit

This register sets a starting pulse rate for varied-speed operation in a range of 1 to 32,767 ($7FFF_{HEX}$) steps. If the parameter is the same as previous, you need not write it anew. In reading the content as 32-bit data, high-place 17 bits are all 0. This register has a preregister function. A parameter written in the preregister R1 is copied to the register R1 at the start.

5.6.3 R2—FH Pulse Rate Register, 15-bit

This register sets an operating pulse rate in a range of 1 to 32,767 ($7FFF_{HEX}$) steps For varied-speed operation, enter a higher value in the register R2 than in the register R1. If the parameter is the same as previous, you need not write it anew. In reading the content as 32-bit data, high-place 17 bits are all 0. This register has a preregister function. A parameter written in the preregister R2 is copied to the register R2 at the start.

5.6.4 R3—Acceleration/Deceleration Rate Register, 16-bit

For varied-speed operation, enter an acceleration rate in a range of 1 to 65,535 (FFFF$_{HEX}$). If the parameter is the same as previous, you need not write it anew. In reading the content as 32-bit data, high-place 16 bits are all 0. This register has a preregister function. A parameter written in the preregister R3 is copied to the register R3 at the start.

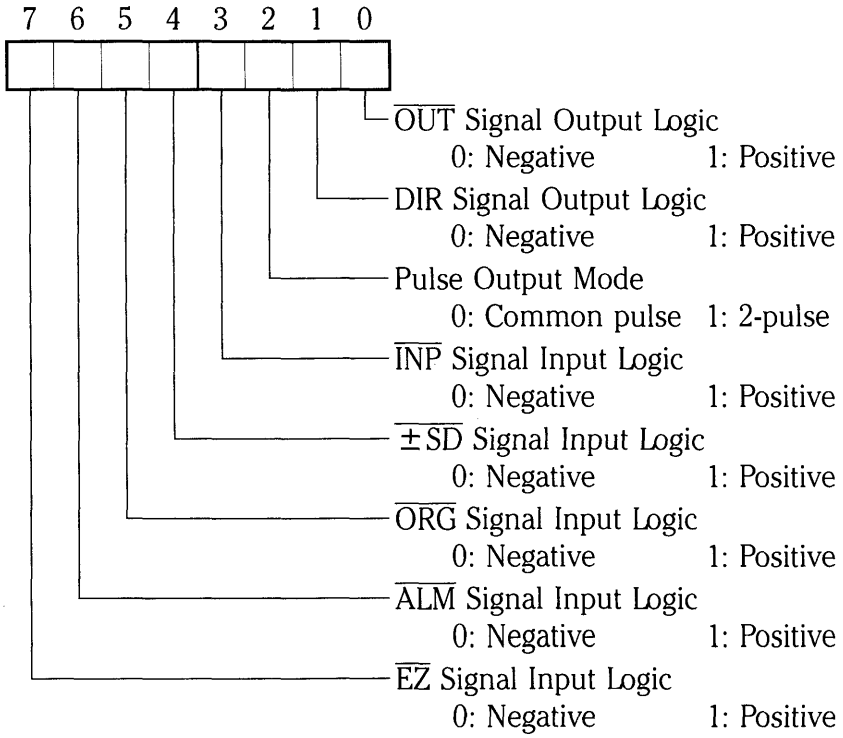
5.6.5 R4—Multiplication Factor Register, 12-bit

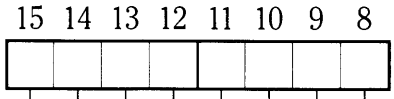
The parameter entered in this register is used to multiply the pulse rates entered in registers Rl and R2. The setting range is 1 to 4,095 (FFF$_{HEX}$). If the parameter is the same as previous, you need not write it anew. In reading the content as 32-bit data, high-place 20 bits are all 0. This register has a preregister function. The parameter written in the preregister R4 is copied to the register R4 at the start.

5.6.6 R5—Ramping-down Point Register, 24-bit

This register sets a starting point of deceleration for varied-speed operation in a preset mode. If the parameter is the same as previous, you need not write it anew. In reading the content as 32-bit data, high-place 8 bits are all 0. This register has a preregister function. The parameter written in the preregister is copied to the register at the start.

5.6.7 R6—Environmental Condition Register 1, 32-bit





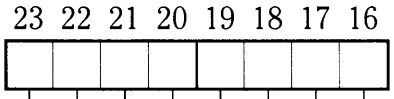
External Input Filter
0: ON 1: OFF

Automatic ERC Signal Output
0: OFF 1: ON

EA and EB Signal Input Mode
00: 1x 90° phase difference signals
01: 2x 90° phase difference signals
10: 4x 90° phase difference signals
11: 2 pulse signals, plus and minus

PA and PB Signal Input Mode
00: 1x 90° phase difference signals
01: 2x 90° phase difference signals
10: 4x 90° phase difference signals
11: 2 pulse signals, plus and minus

ERA and ERB Signal Input Mode
00: 1x 90° phase difference signals
01: 2x 90° phase difference signals
10: 4x 90° phase difference signals
11: 2 pulse signals, plus and minus



Input/Output Selection for BP0
0: Input 1: Ouput

Input/Output Selection for BP1
0: Input 1: Output

Input/Output Selection for BP2
0: Input 1: Output

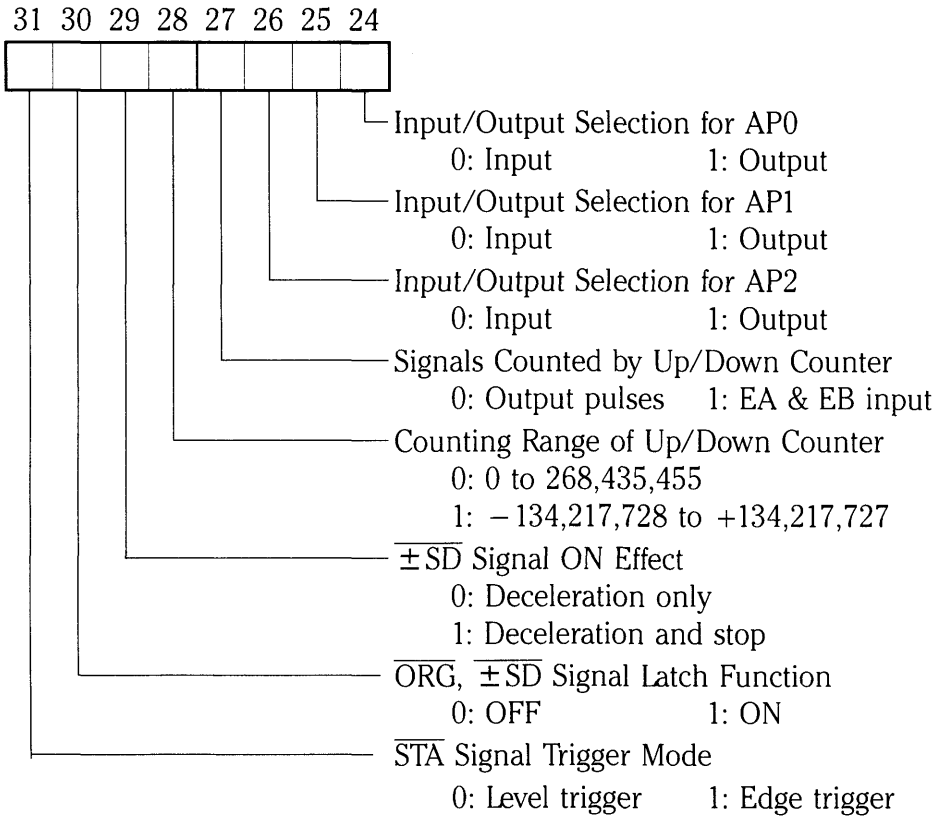
Input/Output Selection for BP3
0: Input 1: Output

Input/Output Selection for BP4
0: Input 1: Output

Input/Output Selection for BP5
0: Input 1: Output

Input/Output Selection for BP6
0: Input 1: Output

Input/Output Selection for BP7
0: Input 1: Output



Bits 7 to 0—Pulse Output Mode

These bits set input/output signal logics and pulse output mode. For details, refer to 5.4.15 Pulse Output Mode.

Bit 8—External Input Filter

To prevent erroneous operation, ±EL, ±SD, ORG, ALM and INP signals are filtered before use in the internal circuit. For quick response, turn the filter off by setting bit 8 at 1. When it is set at 0, input signals with a pulse-width shorter than than 64 cycles at the reference clock (approximately 3μs with a reference clock of 19.6608MHz) are eliminated.

Bit 9—Automatic ERC Signal Output Function

With this function set to ON, the ERC signal is automatically output when the EL or ALM signal stops the PCL5014 from generating pulses or when it completes the origin return.

Bits 11 and 10—EA and EB Signal Input Mode

If you manage the present position according to signals fed back from the encoder, select an input mode for EA and EB pins. If the 2-pulse mode is selected, counting is made at the edge of the signal's changing from low to high level.

Bits 13 and 12—PA and PB Signal Input Mode

If you use a manual pulser or the like for continuous operation, select an input mode for PA and BP pins. If the 2-pulse mode is selected, counting is made at the edge of the signal's changing from low to high level.

Bits 15 and 14—ERA and ERB Signal Input Mode

If you want to detect an out-of-step status based on signals fed back from the encoder, select an input mode for ERA an ERB pins. If the 2-pulse mode is selected, counting is made at the edge of the signal's changing from low to high level.

Bits 23 to 16—Input/Output Selection for BP0 to BP7

Define pins BP0–BP7 as input or output, bit by bit. If the CPU interface is used for a 16-bit bus, settings of bits 23–16 have no function.

Bits 26 to 24—Input/Output Selection of AP2 to AP0

Define pins AP2–AP0 as input or output, bit by bit.

Bit 27—Signals Counted by Up/Down Counter

The up/down counter can count either output pulses or signals input to EA and EB pins. Select either by setting bit 27 at 0 or 1. If the "output pulses" mode is selected, it counts output pulses in the unit number under the microstep control.

Bit 28—Counting Range of Up/Down Counter

A selected counting range does not affect the counting operation. Note, however, that in the preset mode 3 and the zero return mode, processing for calculation of the number of pulses for movement and the comparison method change accordingly.

Bit 29—$\overline{\pm SD}$ Signal ON Effect

Select whether the $\overline{SD}$ signal in the moving direction initiates deceleration only or deceleration and stop. For details, refer to "5.4.14 External Input Signals from Mechanical System."

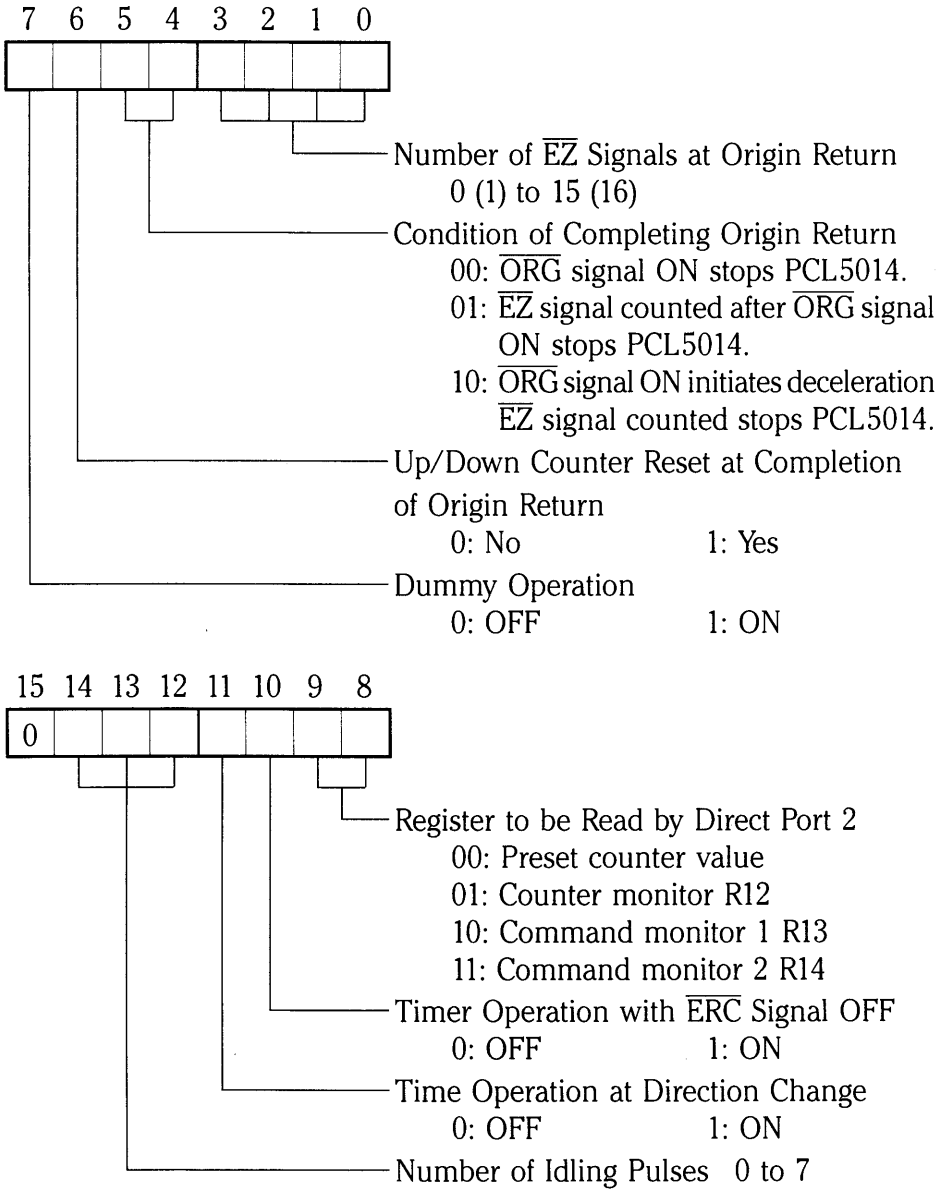
Bit 30—$\overline{ORG}$ and $\overline{\pm SD}$ Signal Latch Function

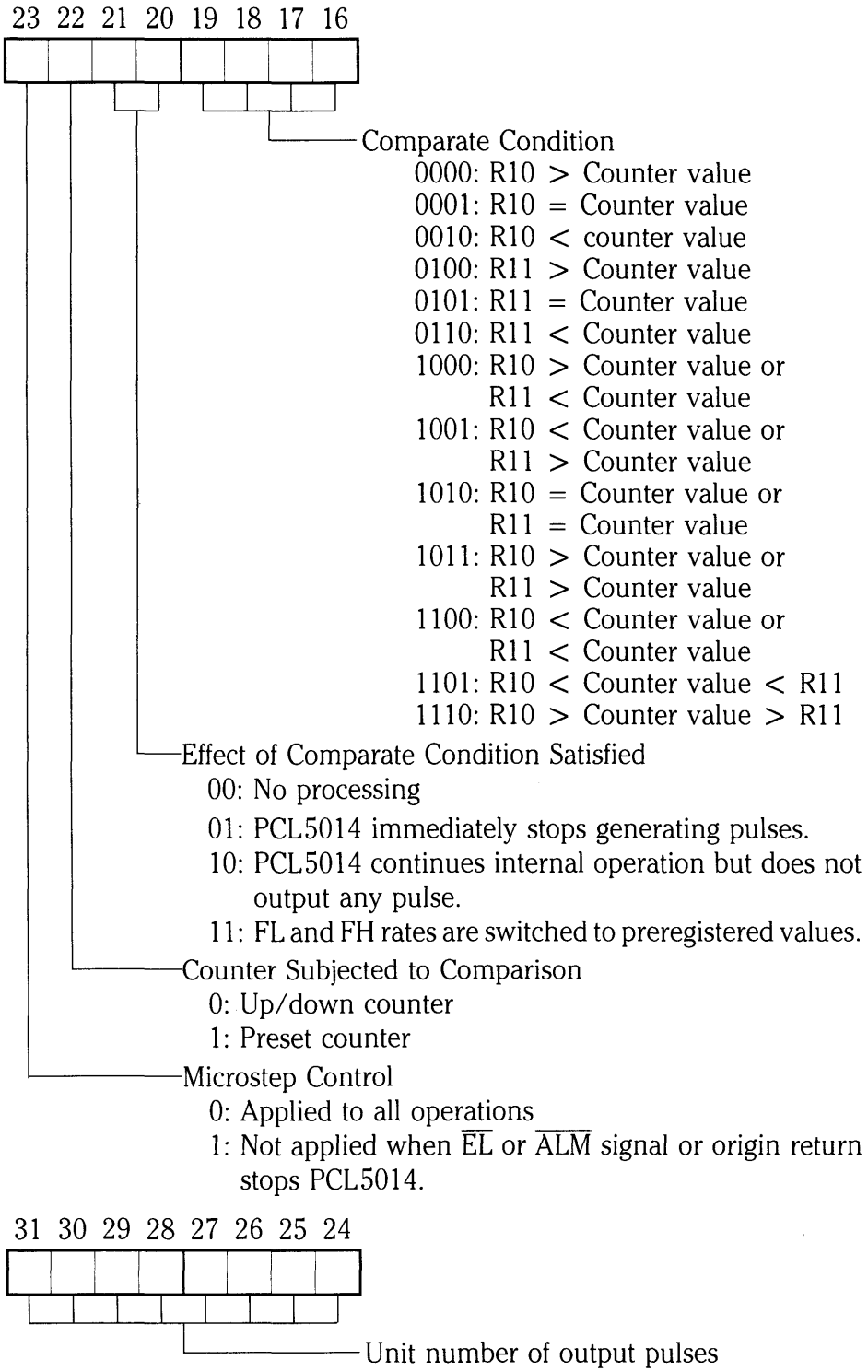
Set the bit at 1. The $\overline{ORG}$ or $\overline{\pm SD}$ signal which is turned from OFF to ON will be internally latched.

Bit 31—$\overline{STA}$ Signal Trigger Mode

Select the simultaneous start signal's trigger mode. Setting the bit at 0 selects the level trigger and setting it at 1 selects the edge trigger. The simultaneous stop signal is fixed to the level trigger.

5.6.8 R7—Environmental Condition Register 2, 32-bit





Bits 3 to 0—Number of $\overline{EZ}$ Signals at Origin Return

If you set bits 5–4 at 01 or 10, the PCL5014 counts the $\overline{EZ}$ signals to complete an origin return. Select the number of counted signals by entering a binary code (required number − 1) in these four bits 3–0.

Bits 5 and 4—Condition to Complete Origin Return

An origin return is available in a simple mode and search mode. In any mode it is completed with the condition selected here.

Bit 6—Up/Down Counter Reset at Completion of Origin Return

Set bit 6 at 1. The up/down counter will be reset upon completion of an origin return.

Bit 7—Dummy Operation

Set bit 7 at 1 when you need to check the operation of PCL5014 without letting it generate any pulse (without moving the target axis). For details, refer to "5.4.12 Dummy Operation."

Bits 9 and 8—Register to be Read by Direct Port 2

You can select a register to directly read the status through the direct port 2. For your reference, you can read the status of up/down counter through the direct port 1.

Bit 10—Timer Operation with $\overline{\text{ERC}}$ Signal OFF

Set bit 10 at 1. Pulse output will be delayed by a time length of 4096 cycles at the reference clock (approximately 200μs with a reference clock of 19.6608MHz) from the $\overline{\text{ERC}}$ signal recovering the OFF status if you will write the start command.

Bit 11—Timer Operation at Direction Change

If the common pulse mode is selected for pulse output, it requires a time for the pulse to be output after the direction signal changes. Set bit 11 at 1, and the start of the next pulse output will be delayed by a time length of 4096 cycles at the reference clock (approximately 200μ with a reference clock of 19.6608MHz) from a change of the DIR signal. In the origin search mode and continuous mode 2, pulse output is alwasys delayed irrespective of this bit setting.

Bits 14 to 12—Number of Idling Pulses

Refer to "5.4.4 Idling Pulse Output."

Bits 19 to 16—Comparator Condition

Select a desired comparator condition by setting bits 19–16.

Bits 21 and 20—Effect of Comparator Condition Satisfied

Refer to "5.4.8 Comparator."

Bit 22—Counter Subjected to Comparison

Select the up/down counter or preset counter, which will be subjected to comparison.

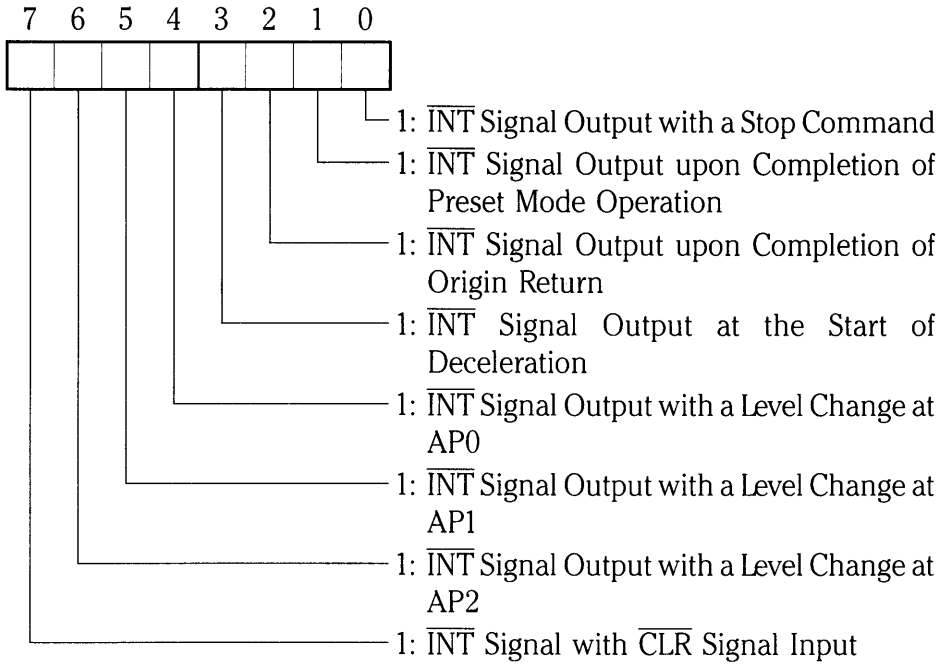
Bit 23—Microstep Control Range

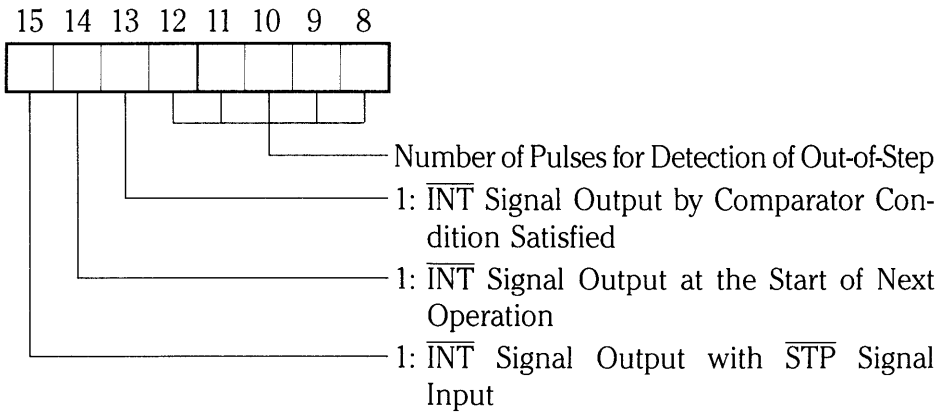
Set bit 23 at 1. The $\overline{\pm\text{EL}}$ or $\overline{\text{ALM}}$ signal or an origin return will stop the PCL5014 from generating pulses in other than the full-step position.

Bits 31 to 24—Unit Number of Output Pulses

Select the unit number of output pulses (resolution of microstep control function). The setting range is 0 to 255 and the unit number is [n (set number) + 1].

5.6.9 R8—Environmental Condition Register 3, 16-bit





Bit 1—INT Signal Output with a Stop Command

Set bit 0 at 1. The INT signal will be output when the immediate stop command or deceleration-stop command will stop the PCL5014 from generating pulses.

Bit 1—INT Signal Output at Completion of Preset Mode Operation

Set bit 1 at 1. The INT signal will be output when the PCL5014 will complete operation in preset modes 1 to 4, zero return mode and one-pulse output mode or when it will complete output of pulses in the designated number in the origin return mode 2.

Bit 2—INT Signal Output at Completion of Origin Return

Set bit 2 at 1. The INT signal will be output when the PCL5014 will complete operation in the origin return mode 1, origin escape mode and origin search mode or when it will stop at the origin in the origin return mode 2.

Bit 4—$\overline{\text{INT}}$ Signal Output at the Start of Deceleration

Set bit 3 at 1. The $\overline{\text{INT}}$ signal will be output at the start of deceleration.

Bit 6 to 4—$\overline{\text{INT}}$ Signal Output with a Level Change at AP0–AP2

Set bit 6, 5 or 4 at 1. The $\overline{\text{INT}}$ signal will be output when the level of pin AP0, AP1 or AP2 will change from high to low level. Input/output selection for these pins has no concern with this operation.

Bit 7—$\overline{\text{INT}}$ Signal Output with $\overline{\text{CLR}}$ Signal Input

Set bit 7 at 1. The $\overline{\text{INT}}$ signal will be output when the $\overline{\text{CLR}}$ signal will change from high to low level to reset the up/down counter.

Bits 12 to 8—Number of Pulses for Detection of Out-of-Step

The PCL5014 judges an out-of-step when an absolute value of the deviation counter for detection of out-of-step exceeds the value set by bits 12–8. The setting range is 0 to 31 pulses. To reset the deviation counter, write the command "62HEX."

Bit 13—$\overline{\text{INT}}$ Signal Output by Comparator Condition Satisfied

Set bit 13 at 1. The $\overline{\text{INT}}$ signal will be output when the comparator condition will be satisfied.

Bit 14—$\overline{\text{INT}}$ Signal Output at the Start of Next Operation

Set bit 14 at 1. The $\overline{\text{INT}}$ signal will be output if parameters will be unsettled for the next operation.

Bit 15—$\overline{\text{INT}}$ Signal with $\overline{\text{STP}}$ Signal Input

Set bit 14 at 1. The $\overline{\text{INT}}$ signal will be output if the next operation is started in unsettled status.

NOTE: If you change setting from 1 to 0 under the condition where the $\overline{\text{INT}}$ signal is ON due to setting at 1, the $\overline{\text{INT}}$ signal recovers the OFF status.

5.6.10 R9—Up/Down Counter Register, 28-bit

This 28-bit binary register retains a current up/down counter value to permit you to manage the present position. Without using any read command, you can read the current up/down counter value through the direct port 1. In reading the status as 32-bit data, high-place four bits are used for a sign if a range of −134,217,728 (8000000HEX) to +134,217,727 (7FFFFFFHEX) is selected by bit 28 of R6. For details, refer to "5.4.7 Up/Down Counter."

5.6.11 R10—Comparator 1 Data Register, 28-bit

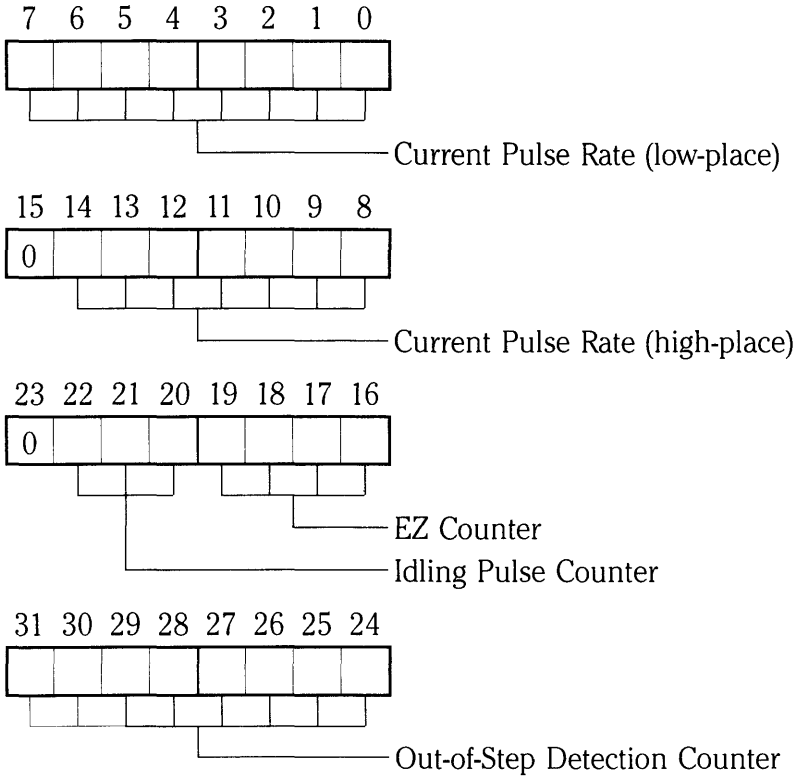
This register retains comparison data for the comparator 1. If the up/down counter is selected for comparison by setting bit 22 of R7 at 0, the setting range for this register is the same as a counting range selected for the up/down counter with bit 28 of R6. If the preset counter is selected for comparison by setting bit 22 of R7 at 1, a setting range for this register is limited to 0 to 268,435,455 (FFFFFFFHEX) only. In reading the status as 32-bit data, high-place four bits are used for a sign if a range of −134,217,728 (8000000HEX)

to +134,217,727 (7FFFFFFHEX) is selected. For details, refer to "5.4.8 Comparator."

5.6.12 R11—Comparator 2 Data Register, 28-bit

This register retains comparison data for the comparator 2 with the same manner as the R10 register.

5.6.13 R12—Counter Monitor, 32-bit



Bits 15 to 0—Current Pulse Rate

These bits allow you to monitor the current pulse rate in steps (the same steps as retained in registers R1 and R2) used for acceleration, deceleration, etc. Note, however, that during cessation of pulse output these bits indicate the pulse rate retained in the FL register R1.

Bits 19 to 16—EZ Counter

These bits allow you to monitor the EZ counter value used for origin return. Until the counting condition is satisfied, they indicate the set number of $\overline{EZ}$ signals and when the condition is satisfied, each $\overline{EZ}$ signal lets the counter count down. After counting down to 0, it recovers the initial value.

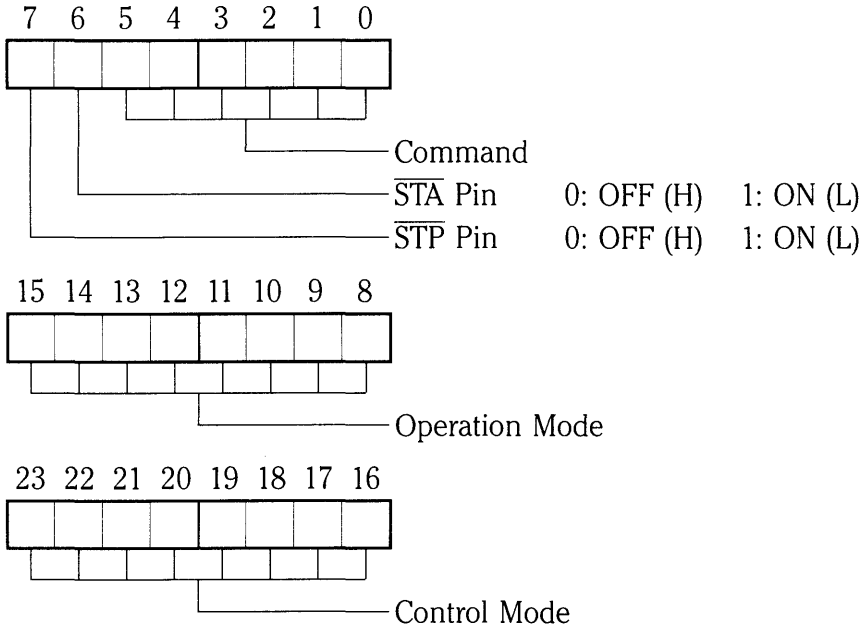
Bits 22 to 20—Idling Pulse Counter

Bits 22–20 allow you to monitor the idling pulse counter. During cessation of pulse output, these bits indicate the set number of idling pulses and when the PCL5014 starts outputting pulses, it counts down idling pulses. Counting down to 0 starts accleration. Under the microstep control, acceleration starts after pulses are output in the number multiplied by the unit number.

Bits 29 to 24—Out-of-Step Detection Counter

Bits 29–24 allow you to monitor a current value of the out-of-step detection counter. If the value is negative, it is read as a twos complement. Though the counter is of 6 bits, you can read the data in 8 bits with an extension for a sign. If the motor is in a minus direction from the position integrated by output pulses, the counter value is positive and if the motor is in a plus direction from the integrated position, the counter value is negative.

5.6.14 R13—Command Monitor 1, 24-bit



Bits 5 to 0—Command

These bits allow you to monitor the low-place 6 bits of the last command among those written at the cessation of pulse output (00HEX to 30HEX).

Bits 7 and 6—$\overline{\text{STA}}$ and $\overline{\text{STP}}$ Pins

These bits allow you to monitor the status of $\overline{\text{STA}}$ and $\overline{\text{STP}}$ pins.

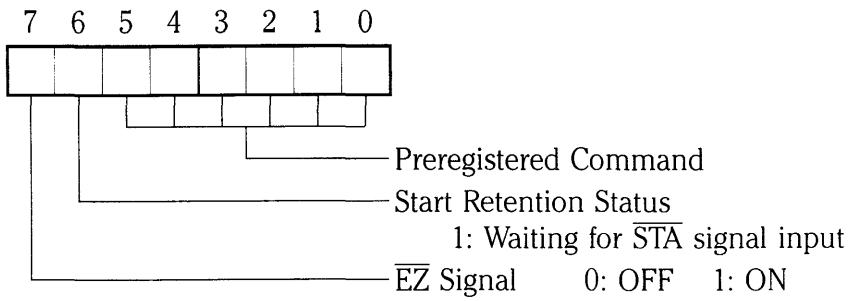
Bits 15 to 8—Operation Mode

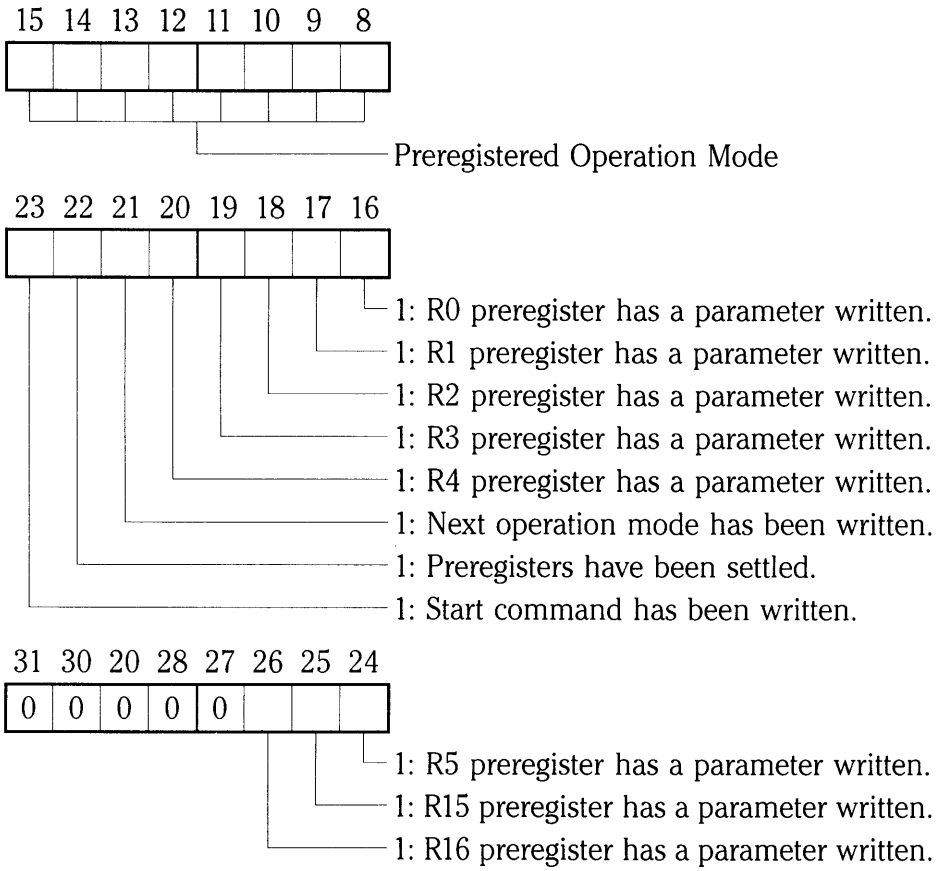
These bits allow you to monitor the present operation mode.

Bits 23 to 16—Control Mode

These bits allow you to monitor the present control mode.

5.6.15 R14—Command Monitor 2, 27-bit





Bits 5 to 0—Preregistered Command

These bits allow you to monitor low-place 6 bits of a start command for the next operation. (High-place 2 bits are 00.)

Bit 6—Start Retention Status

This bit keeps indicating "1" from receiving the start retention command to inputting the $\overline{\text{STA}}$ signal.

Bit 7—$\overline{\text{EZ}}$ Signal

This bit allows you to monitor the ON/OFF status of the signal according to the input logic.

Bits 15 to 8—Preregistered Operation Mode

These bits allow you to monitor the preregistered next operation mode.

Bits 20 to 16 and 26 to 24—Preregister Written Status

These bits indicates "1" when preregisters R0 to R5, R15 and R16 have parameters written. Starting the next operation lets all these bits indicate 0.

Bit 21—Next Operation Mode

This bit indicates "1" when the next operation mode is written. Starting the next operation lets the bit indicate 0.

Bit 22—Preregister Settled Status

This bit indicates "1" when you write a start command or settled command (66HEX) during operation with bit 4 of the control mode bufer at

1. Starting the next operation, writing an unsettled command (67HEX), writing a stop command (09HEX, 0AHEX) or abnormal stop lets the bit indicate 0. With this bit set at 1, completion of the present operation starts the next operation automatically.

Bit 23—Start Command Written

This bit indicates "1" when a start command is written and "0" when the PCL5014 stops pulse output. A difference from status bit 2 ($\overline{\text{BSY}}$ pin monitor of the status buffer is that the start retention status (waiting for the $\overline{\text{STA}}$ signal) lets this bit indicate 1 while bit 2 of the status buffer indicates 0 (cessation).

5.6.16 R15—Deceleration Rate Register, 16-bit

This register sets the deceleration rate for the varied-speed operation in a range of 1 to 65,535 (FFFFHEX). If the parameter is the same as previous, you need not set anew. In reading the parameter in 32-bit data, high-place 16 bits are all 0.

The register has a preregister function. The parameter written in the preregister is copied to the register at the start. If 0 (default) is written in the register, the acceleration rate written in the R3 register is used for deceleration.

5.6.17 R16—S-curve Related Parameter Register, 14-bit

The register R16 sets the S-curve related parameter in the number of pulse steps to put an intermediate linear acceleration/deceleration on the way of acceleration/deceleration. If the acceleration/deceleration time is fixed, an intermediate linear acceleration/deceleration allows you to lower the maximum acceleration rate.

A resultant acceleration/deceleration pattern is that S-curve acceleration/deceleration applies between the FL pulse rate to (FL pulse rate + R16) pulse rate and between (FH pulse rate − R16) pulse rate to the FH pulse rate, while an intermediate linear acceleration/deceleration applies in between. If the R16 is set at 0 (default), (FH − FL)/2 is used as the S-curve related parameter.

5.7 Monitor

You can check the following by monitoring the status code.

(1) Status

Pulse output: Stopping, accelerating, operating at a constant rate, decelerating, timer operating to delay the start

Signals: $\overline{\pm EL}$, $\overline{\pm SD}$, $\overline{ORG}$, $\overline{CMP}$, $\overline{ALM}$, $\overline{ERC}$, $\overline{INP}$, $\overline{EZ}$, $\overline{CLR}$, $\overline{BSY}$

Input/output status of general-purpose I/O ports AP0, AP1 and AP2

(2) Interrupt Status

You can read the factor which causes the $\overline{INT}$ signal to be output.

(3) Input/Output Status of General-purpose I/O Ports BP0 to BP7

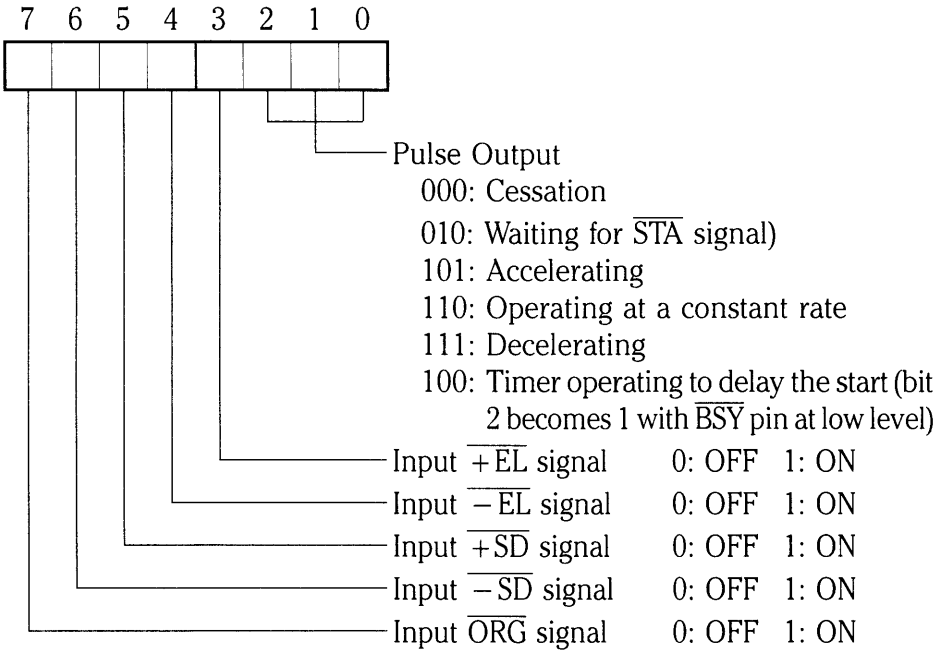
(4) Parameters Retained in Registers

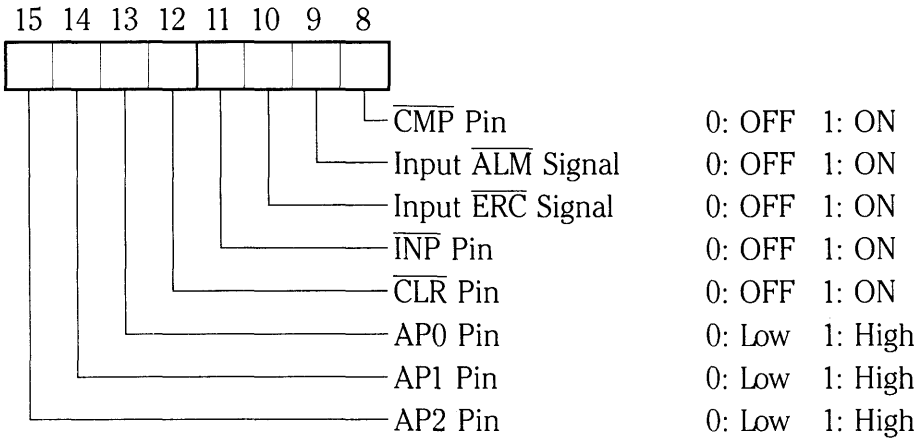
(5) Direct Reading of Parameters Retained in Registers

(Preset counter, R12, R13 and R14 through the direct port 2; up/down counter through the direct port 1)

5.7.1 Status

The conditions at the start of processing for status reading are latched. So contents in the data bus do not change during the read cycle. But if you read the status successively, allow a time length of over two cycles at the reference clock (approximately 0.1 μs with a reference clock of 19.6608MHz) for the $\overline{CS}$ pin to become high level.





Bits 2 to 0—Pulse Output

You can check the present status of pulse output. "100" indicates that the ERC signal is being output, the timer is operating to stop pulse output until the ERC signal recovers the OFF status, the timer is operating to meet pulse output with a direction change in the common pulse mode, or the INP signal is waited for. (For details, refer to bits 10 and 11 of R7—Environmental Condition Setting Register (6.6.8).)

Bits12 to 3—±EL, ±SD, ORG, CMP, ALM, ERC, INP, EZ and CLR Signals

You can check the input/output status of these signals with ON/OFF conditions based on the input logic.

Bits 15 to 13—General-purpose I/O Ports

You can monitor the status of general-purpose I/O ports whether they are defined as input or output.

6. Hardware

6.1 Terminal Pin Assignment

Pin No.	Name	Input/Output	Logic	Description
1	$\overline{CS}$	I	Negative	Chip select signal
2	$\overline{RD}$ (E)	I	Negative	Read signal
3	$\overline{WR}$ (R/$\overline{W}$)	I	Negative	Write signal
4	$\overline{US}$	I	Negative	High-place data (D8 to D15) select signal
5	A0 ($\overline{LS}$)	I	Positive	Address bus signal 0 (low-place data select signal)
6	A1	I	Positive	Address bus signal 1
7	A2	I	Positive	Address bus signal 2
8	A3	I	Positive	Address bus signal 3
9	D0	I/O	Positive	Data bus signal 0
10	GND	I		Ground
11	D1	I/O	Positive	Data bus signal 1
12	D2	I/O	Positive	Data bus signal 2
13	D3	I/O	Positive	Data bus signal 3
14	D4	I/O	Positive	Data bus signal 4
15	D5	I/O	Positive	Data bus signal 5
16	D6	I/O	Positive	Data bus signal 6
17	D7	I/O	Positive	Data bus signal 7
18	D8 (BP0)	I/O	Positive	Data bus signal 8 (general-purpose port)
19	D9 (BP1)	I/O	Positive	Data bus signal 9 (general-purpose port)
20	D10 (BP2)	I/O	Positive	Data bus signal 10 (general-purpose port)
21	D11 (BP3)	I/O	Positive	Data bus signal 11 (general-purpose port)
22	D12 (BP4)	I/O	Positive	Data bus signal 12 (general-purpose port)
23	D13 (BP5)	I/O	Positive	Data bus signal 13 (general-purpose port)
24	D15 (BP6)	I/O	Positive	Data bus signal 14 (general-purpose port)
25	D15 (BP7)	I/O	Positive	Data bus signal 15 (general-purpose port)
26	Vdd	I		+5V ±5%
27	AP0	I/O	Positive	Universal port
28	AP1	I/O	Positive	Universal port
29	AP2	I/O	Positive	Universal port
30	GND	I		Ground
31	$\overline{CLR}$	I*	Negative	Clears the up/down counter.
32	EA	I*		Encoder A phase signal, up signal
33	EB	I*		Encoder B phase signal, down signal
34	$\overline{EZ}$	I*	Negative***	Encoder Z phase signal

Pin No.	Name	Input/Output	Logic	Description
35	PA	I*		Manual pulser A phase signal
36	PB	I*		Manual pulser B phase signal
37	ERA	I*		Encoder A phase signal for out-of-step detection
38	ERB	I*		Encoder B phase signal for out-of-step detection
39	$\overline{\text{ALM}}$	I*	Negative***	Servo alarm signal (immediate stop)
40	$\overline{\text{INP}}$	I*	Negative***	Servomotor in-position signal
41	$\overline{\text{ERC}}$	I/O**	Negative	Clears the deviation counter.
42	GND	I		Ground
43	$\overline{\text{OUT}}$	O	Negative***	Output pulse/output pulse to (+) direction
44	DIR	O	H***	Direction signal/output pulse to (−) direction
45	$\overline{+\text{EL}}$	I*	Negative	Mechanical (+) direction end limit signal
46	$\overline{-\text{EL}}$	I*	Negative	Mechanical (−) direction end limit signal
47	$\overline{+\text{SD}}$	I*	Negative***	Mechanical (+) direction ramping-down signal
48	$\overline{-\text{SD}}$	I*	Negative***	Mechanical (−) direction ramping-down signal
49	$\overline{\text{ORG}}$	I*	Negative***	Mechanical origin return signal
50	$\overline{\text{STA}}$	I/O**	Negative	Simultaneous start signal
51	$\overline{\text{STP}}$	I/O**	Negative	Simultaneous stop signal
52	$\overline{\text{CMP}}$	O	Negative	Comparate condition satisfied
53	$\overline{\text{BSY}}$	O	Negative	Operation monitor signal (operation in progress)
54	$\overline{\text{FUP}}$	O	Negative	Operation monitor signal (ramping-up)
55	$\overline{\text{FDW}}$	O	Negative	Operation monitor signal (ramping-down)
56	I/$\overline{\text{M}}$	I*		CPU interface switchover to Intel or Motorola
57	B/$\overline{\text{W}}$	I*		CPU interface switchover to 8 or 16 bits
58	Vdd	I		+5V ±5%
59	Vdd	I		+5V ±5%
60	CLK	I		Reference clock
61	GND	I		Ground
62	$\overline{\text{RST}}$	I	Negative	Internal reset signal
63	$\overline{\text{INT}}$	O**	Negative	Interrupt request signal
64	$\overline{\text{WRQ}}$	O	Negative	Wait request signal for access to CPU

*: With pull-up resistor

**: With pull-up resistor and connectable in wired OR

***: The logic is changeable and the indicated one is the default logic.

H: The default condition is high level.

6.2 Terminal Pin Functions (Pin No. in brackets)

6.2.1 Vdd [26, 58, 59], GND [10, 30, 42, 61]

These are power input pins. Be sure to input +5V ±5% to all Vdd pins and connect all GND pins to the ground.

6.2.2 CLK [60]

This pin is reference clock input. You are recommended to use a reference clock of 19.6608MHz. The PCL3013 produces output pulses referring to the clock. Accordingly, the accuracy of output pulses depends on the clock. The reference clock is also used for internal control.

6.2.3 $\overline{\text{RST}}$ [62]

The PCL3013 is reset if the reference clock is input in over eight cycles with this pin placed in low level. For reset conditions, refer to "4.5 Default (Reset) Conditions of PCL3013."

6.2.4 $\overline{\text{CS}}$ [1]

Placing this pin in low level enables $\overline{\text{RD}}$ and $\overline{\text{WR}}$ pins.

6.2.5 $\overline{\text{RD}}$ (E) [2]

This pin is active when the $\overline{\text{CS}}$ pin is low level. It inputs the $\overline{\text{RD}}$ signal for the Intel system or the E signal in the case of 8-bit or Motorola system.

6.2.6 $\overline{\text{WR}}$ (R/$\overline{\text{W}}$) [3]

This pin is active when the $\overline{\text{CS}}$ pin is low level. It inputs the $\overline{\text{WR}}$ signal in the case of Intel system or the R/$\overline{\text{W}}$ signal in the case of Motorola system.

6.2.7 $\overline{\text{WRQ}}$ [64]

Command processing requires four cycles of the reference clock. This pin outputs the signal to let the CPU wait if the PCL3013 is accessed from the CPU during command processing in these four cycles at the reference clock.

6.2.8 $\overline{\text{US}}$ [4]

This pin is active when the $\overline{\text{CS}}$ pin is low level. The signal selects high-place 8 bits of the 16-bit data bus.

6.2.9 A0 to A3 [5 to 8]

These pins input address signals. If the PCL3013 is connected to the 16-bit data bus, the signal at A0 pin selects low-place 8 bits of the 16-bit data bus.

6.2.10 D0 to D7 [9, 11 to 17]

These pins form a bidirectional data buse, which is connected to low-place 8 bits if the 16-bit data bus is connected.

6.2.11 D8 to D15 [18 to 25]

These pins are connected to high-place 8 bits when the 16-bit data bus is used. They are universal I/O pins BP0 to BP7 when the 8-bit data bus is used. Under the default condition, they are input ports but you can define each individual bit as an output port with a software technic. Since the PCL5014 is a CMOS LSI, pull up unused pins using external resistors of 1kΩ to 100kΩ.

6.2.12 I/$\overline{M}$ [56] and B/$\overline{W}$ [57] with Pull-up Resistor

These pins select types of the interface to the CPU.

6.2.13 $\overline{INT}$ [63]

This pin outputs an interrupt request signal to the CPU. If you use two or more units of PCL5014, you can connect them in a wired OR mode. When it reads the interrupt status after outputting the signal, this pin is turned off. The pin requires an external pull-up resistor of 5kΩ to 10kΩ.

6.2.14 $\overline{+EL}$ [45] and $\overline{-EL}$ [46] with Pull-up Resistor

The $\overline{+EL}$ pin detects an end limit signal for the plus direction and the $\overline{-EL}$ pin detects an end limit signal for the minus direction. You can check their ON/OFF condition by monitoring the status.

6.2.15 $\overline{+SD}$ [47] and $\overline{-SD}$ [48] with Pull-up Resistor

The $\overline{+SD}$ pin detects a ramping-down signal for the plus direction and the $\overline{-SD}$ pin detects a ramping-down signal for the minus direction. You can change or mask the input logic with a software technic and check their ON/OFF condition by monitoring the status.

6.2.16 $\overline{ORG}$ [49] with Pull-up Resistor

This pin inputs an origin return signal. You can change the input logic with a software technic and check the ON/OFF condition by monitoring the status.

6.2.17 $\overline{OUT}$ [43]

This pin can output two types of signal. In the common pulse mode, it outputs the pulse of which the direction depends on the DIR signal. In the 2-pulse mode, it outputs pulses in the plus direction. You can change or mask the output logic with a software technic.

6.2.18 DIR [44]

This pin can output two types of signal in conjunction with the $\overline{OUT}$ pin. In the common pulse mode, it outputs a direction signal. In the 2-pulse mode, it outputs pulses for the minus direction. You can change the output logic with a software technic. In the 2-pulse mode, you can mask the output if required.

6.2.19 EA [32] and EB [33] with Pull-up Resistor

These are encoder input pins for up/down counter. They can also input 90° phase difference signals (1, 2 or 4 times multiplied) or 2 pulse signals (plus and minus). In the case of inputting 90° phase difference signals, the up/down counter counts up if the phase of EA signal leads the EB signal. For 2-pulse signals, the EA pin inputs the plus pulse and the EB pin inputs the minus pulse.

6.2.20 $\overline{EZ}$ [34] with Pull-up Resistor

This is the input for encoder marker pulse $\overline{EZ}$. The $\overline{EZ}$ signal is used in origin return, origin search and origin escape modes. This signal improves the accuracy of origin return. You can change the input logic with a software technic and read the input status with the register R14.

6.2.21 PA [35] and PB [36] with Pull-up Resistor

These pins input external pulse signals. In the continuous mode 2 or the preset mode 4, inputting external pulse signals to these pins lets the $\overline{OUT}$ and DIR pins output the pulses. In the continuous mode 2, the moving direction is determined by PA and PB signals, while in the preset mode 4, the direction is as set by the CPU. You can input 90° phase difference signals (1, 2 or 4 times multiplied) to these pins or a plus pulse to the PA pin and a minus pulse to the PB pin. In the case of inputting 90° phase difference signals, the moving direction is plus if the phase of PA signal advances over the PB signal. You can use a pulser (manual revolution encoder) to input pulses to these pins.

6.2.22 ERA [37] and ERB [38] with Pull-up Resistor

These pins receive signals from the encoder for detection of an out-of-step condition of stepping motor. You can input 90° phase difference signals (1, 2 or 4 times multiplied) to these pins or a plus pulse to the ERA pin and a minus pulse to the ERB pin. In the case of 90° phase difference signals, input them in such a manner that the phase of ERA signal advances over the ERB signal when operating in the plus direction.

6.2.23 $\overline{ALM}$ [39] with Pull-up Resistor

This pin inputs an external alarm signal, which immediately stops the PCL5014 from outputting pulses. Also, when the signal is on, writing a start command does not start the PCL5014 outputting any pulse. Whether the PCL5014 is outputting pulses or not, inputting the $\overline{ALM}$ signal to this pin lets the PCL5014 output the $\overline{INT}$ signal. You can change the input logic with a software technic and check the ON/OFF condition by monitoring the status.

6.2.24 $\overline{\text{INP}}$ [40] with Pull-up Resistor

This pin receives an in-position signal from the servo driver. You can change the input logic with a software technic and check the ON/OFF condition by monitoring the status.

6.2.25 $\overline{\text{ERC}}$ [41]

This pin outputs the signal to reset the deviation counter of servo driver. The pulseswidth of the output signal is 4096 cycles at the reference clock (approximately 200μs with a reference clock of 19.6608MHz). If you do not use the pin, place it in an open condition. Also note that the pin requires an external pull-up resistor of 5kΩ to 10kΩ.

6.2.26 $\overline{\text{STA}}$ [50]

If you use two or more units of PCL5014 to control multiple axes, connect the $\overline{\text{STA}}$ pins of all units, and the $\overline{\text{STA}}$ signal will simultaneously start all axes. If connected to such the effect, you can set the system with a software technic so that the $\overline{\text{STA}}$ signal starts some specific axis only. You can also start all axes simultaneously by sending an external signal. When you write the simultaneous start command, the pin outputs a pulse signal with a time width of 512 cycles at the reference clock (approximately 26μs with a reference clock of 19.6608MHz). You can read the ON/OFF condition with the R13 register. If you do not use the pin, place it in an open condition.

6.2.27 $\overline{\text{STP}}$ [51]

If you use two or more units of PCL5014, connect the $\overline{\text{STP}}$ pins of all units. All units will simultaneously stop outputting pulses if some unit stops generating pulses due to an abnormal event. When a factor to simultaneously stop all units is generated, this pin outputs a pulse signal with a time width of 512 cycles at the reference clock (approximately 26μs with a clock of 19.6608MHz). If connected to such the effect, you can set the system so that the $\overline{\text{STP}}$ signal may not stop all units except for the unit causing the signal. You can also stop all axes simultaneously by sending an external signal. When the $\overline{\text{STP}}$ pin is at a low level, writing a start command does not start the the PCL5014 outputting pulses. You can check the ON/OFF condition with the R13 register. If you do not use this pin, place it in an open condition.

6.2.28 AP0 to AP2 [27 to 29]

These pins are general-purpose input/output ports. You can individually set each pin to input or output. You can also let these pins output the $\overline{\text{INT}}$ signal by inputting the signal. If you do not use these pins, connect external pull-up resistors of 1kΩ to 100kΩ.

6.2.29 $\overline{\text{CLR}}$ [31] with Pull-up Resistor

This pin clears the up/down counter by changing from high to low level, though counting is made under the low level condition. The $\overline{\text{INT}}$ signal can be output when clearing the counter. You can check the ON/OFF condition by monitoring the status.

6.2.30 $\overline{\text{CMP}}$ [52]

This pin becomes low level while the comparator condition is being satisfied. You can check the ON/OFF condition by monitoring the status.

6.2.31 $\overline{\text{BSY}}$ [53]

This pin becomes high level when the PCL5014 stops outputting pulses and becomes low level when it is outputting pulses. The $\overline{\text{INP}}$ signal delays the output timing. You can check the ON/OFF condition by monitoring the status.

6.2.32 $\overline{\text{FUP}}$ [54]

This pin becomes low level during ramping-up.

6.2.33 $\overline{\text{FDW}}$ [55]

This pin becomes low level during ramping-down.

6.3 CPU Interface Function

The PCL5014 is so designed that you can connect it to the Intel or Motorola CPU of 8 or 16 bits by setting I/M and B/W pins as follows.

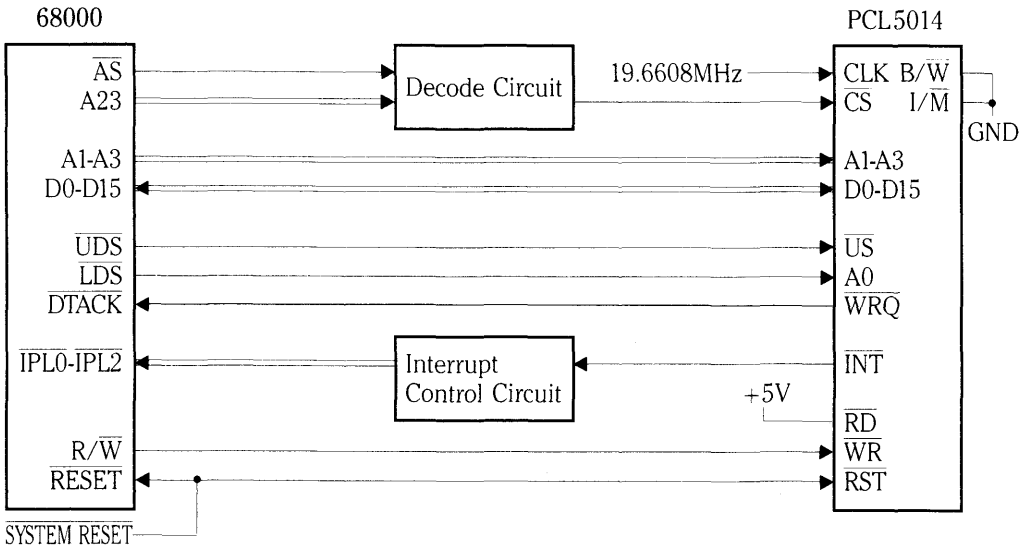
CPU	I/$\overline{\text{M}}$ Pin	B/$\overline{\text{W}}$ Pin	Interface Specifications
68000	L	L	Motorola 16-bit CPU
6809	L	H	Motorola 8-bit CPU
8086	H	L	Intel 16-bit CPU
Z80	H	H	Intel 8-bit CPU

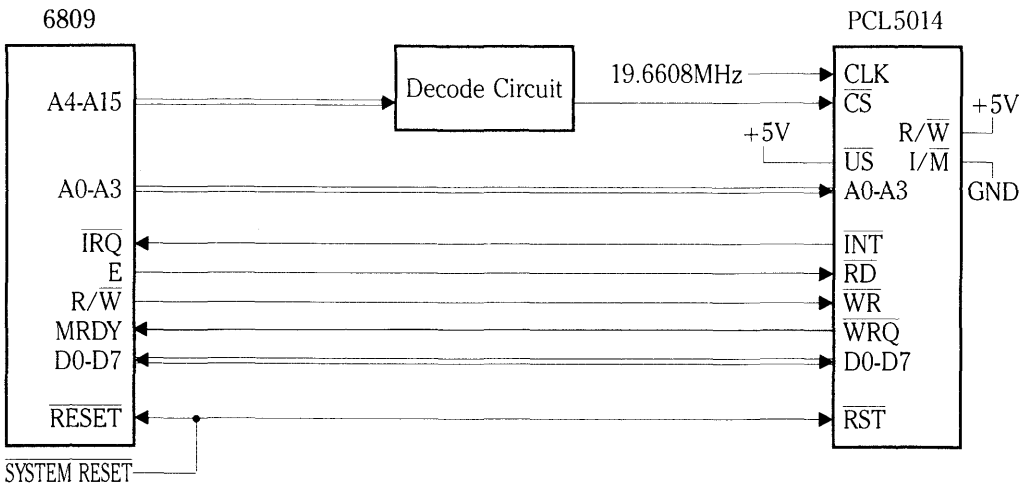
Connect CPU signals as follows.

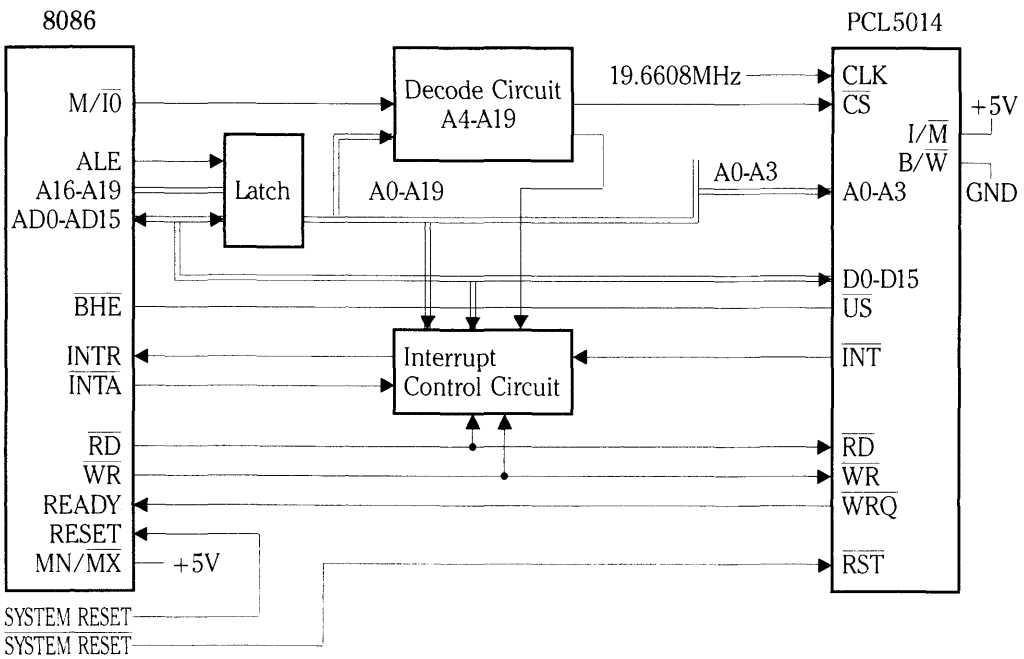
CPU	Terminal Pins on PCL5014							
	$\overline{\text{RD}}$	$\overline{\text{WR}}$	A3	A2	A1	A0	$\overline{\text{US}}$	$\overline{\text{WRQ}}$
68000	+5V	R/$\overline{\text{W}}$	A3	A2	A1	$\overline{\text{LDS}}$	$\overline{\text{UDS}}$	$\overline{\text{DTACK}}$
6809	E	R/$\overline{\text{W}}$	A3	A2	A1	A0	+5V	MRDY
8086	$\overline{\text{RD}}$	$\overline{\text{WR}}$	A3	A2	A1	A0	$\overline{\text{BHE}}$	READY
Z80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	A3	A2	A1	A0	+5V	$\overline{\text{WAIT}}$

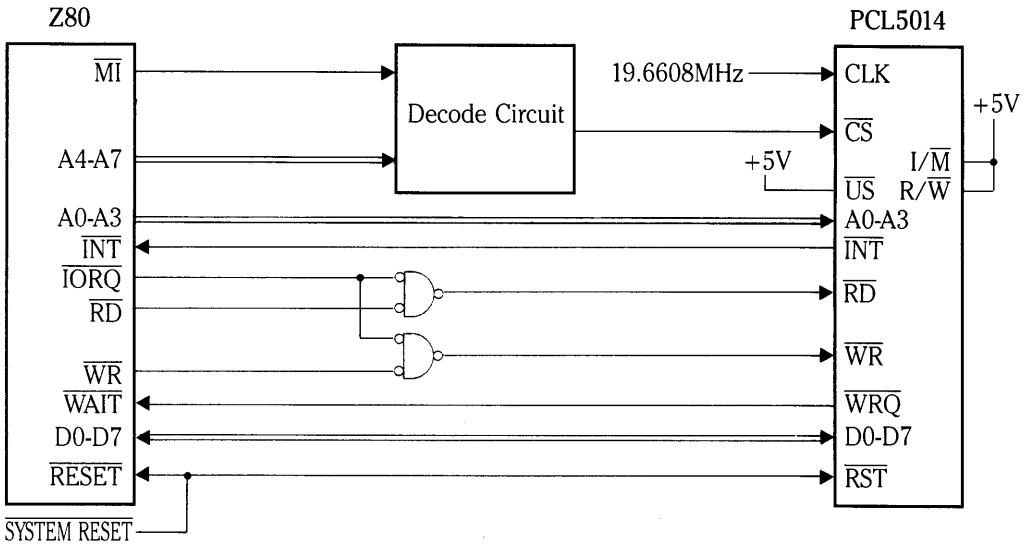
NOTE: By connecting the A3 pin to the ground, you can secure the address space to the eighth address. Note, however, that such connection voids the direct reading function for the up/down counter, etc. and reading will be all made through the input/output buffer.

6.4 Block Diagrams of CPU Interface Circuit









6.5 Precautions in Designing Hardware

- Notice that the CLK pin only operates at the CMOS level.
- Allow a time length of over eight cycles at the reference clock for the $\overline{RST}$ signal at low level.
- Using a resistor of 1kΩ to 100kΩ, pull up any of pins AP0 to AP2 which will not be used.
- If you connect the PCL5014 to the CPU via the 8-bit bus, you may use pins D8 to D15 as general-purpose I/O pins. But if you do not use these pins, pull up them with resistors of 1kΩ to 100kΩ.
- If you connect the PCL5014 to the CPU via the 8-bit bus, connect the $\overline{US}$ pin to Vdd.
- Connect the $\overline{RD}$ pin to Vdd if the B/$\overline{W}$ pin is low level when the I/$\overline{M}$ pin is low level (68000 mode).
- For safety the input logic of $\overline{+EL}$ and $\overline{-EL}$ pins cannot be changed. If you need to change the input logic, prepare an external circuit for such the purpose.
- Though $\overline{INT}$ and $\overline{ERC}$ pins have a pull-up resistor built in, you need to additionally mount an external pull-up resistor of 5kΩ to 10kΩ, since their resistance is high.

7. Characteristics

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Voltage	V_{dd}	−0.3 to +7.0	V
Input Voltage	V_{IN}	−0.3 to V_{dd} +0.3	V
Input Current	I_{IN}	±10	mA
Storage Temperature	T_{stg}	−40 to +125	°C

7.2 Recommended Operating Conditions

Item	Symbol	Rating	Unit
Power Voltage	V_{dd}	4.75 to 5.25	V
Ambient Temperature	T_J	0 to +70	°C

7.3 DC Characteristics

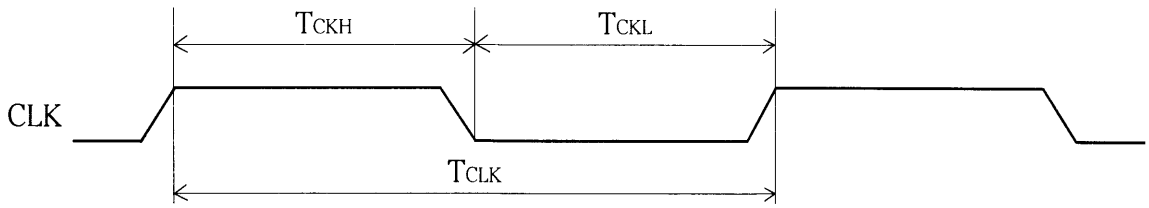
Item	Symbol	Condition	Min.	Max.	Unit
Static Current Consumption	I_{dd1}	CLK = 0Hz		100	μA
Current Consumption	I_{dd2}	Note 1		44	mA
Output Leakage Current	I_{OZ}	Note 2	−10	10	μA
		Note 3	−200	10	μA
Input Capacity				2.3	pF
Low Level Input Current	I_{IL}	Note 4	−10	10	μA
		Note 5	−200	−10	μA
High Level Input Current	V_{IH}		−10	10	μA
Low Level Input Voltage	V_{IL}	Note 6		0.8	V
		Note 7		1.0	V
High Level Input Voltage	V_{IH}	Note 6	2.2		V
		Note 7	4.0		V
Low Level Output Current	I_{OL}	Notes 2 and 3		8	mA
High Level Output Current	I_{OH}	Note 2		−8	mA
Low Level Output Voltage	V_{OL}	I_{OL} = 1μA		0.05	V
		I_{OL} = 8mA		0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = −1μA	V_{dd} − 0.05		V
		I_{OH} = −8mA	2.4		V
Internal Pull-up Resistance	R_{UP}		25	500	kΩ

NOTES: 1. CLK = 19.6608MHz, output frequency = 4.9152MHz, with no load
2. D0–D15, I/O8–I/O10. $\overline{OUT}$, DIR, $\overline{CMP}$, $\overline{BSY}$, $\overline{FUP}$, $\overline{FDW}$
3. $\overline{ERC}$, $\overline{STA}$, $\overline{STP}$, $\overline{INT}$, $\overline{WRQ}$
4. $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{US}$, A0–A3, D0–D15, CLK, $\overline{RST}$
5. $\overline{CLR}$, EA, EB, $\overline{EZ}$, PA, PB, ERA, ERB, $\overline{ALM}$, $\overline{INP}$, $\overline{ERC}$, $\overline{+EL}$, $\overline{-EL}$, $\overline{+SD}$, $\overline{-SD}$, $\overline{ORG}$, $\overline{STA}$, $\overline{STP}$, I/$\overline{M}$, B/$\overline{W}$
6. Input of other than CLK and input/output pins
7. CLK pin only

7.4 AC Characteristics

7.4.1 Reference Clock

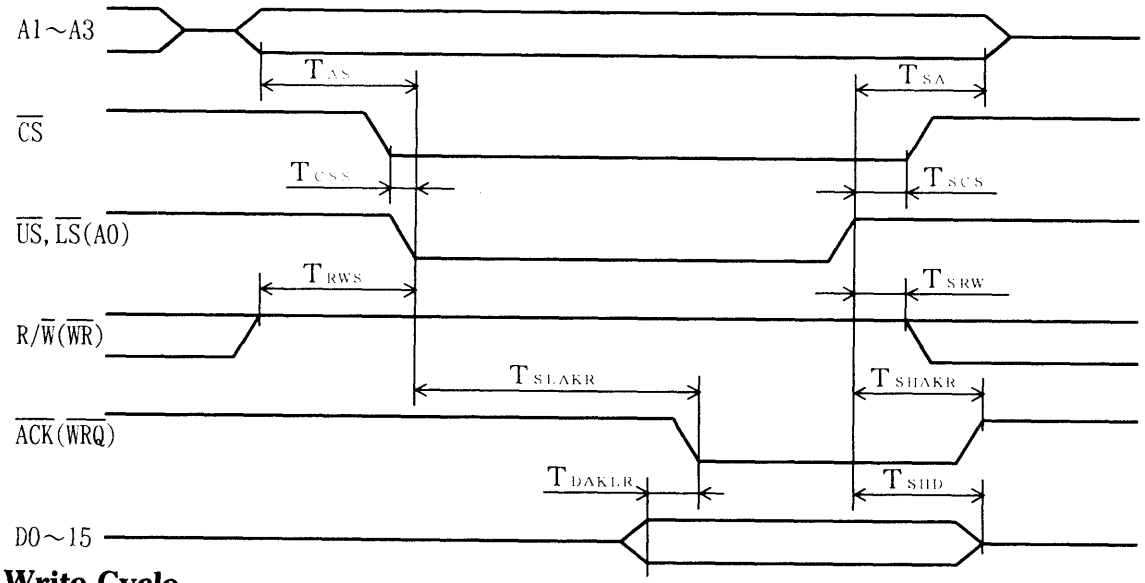
Item	Symbol	Condition	Min.	Max.	Unit
Reference Clock Frequency	f_{CLK}			25	MHz
Cycle Time at Reference Clock	T_{CLK}		40		ns
Time Width of High Level	T_{CKH}		20		ns
Time Width of Low Level	T_{CKL}		20		ns



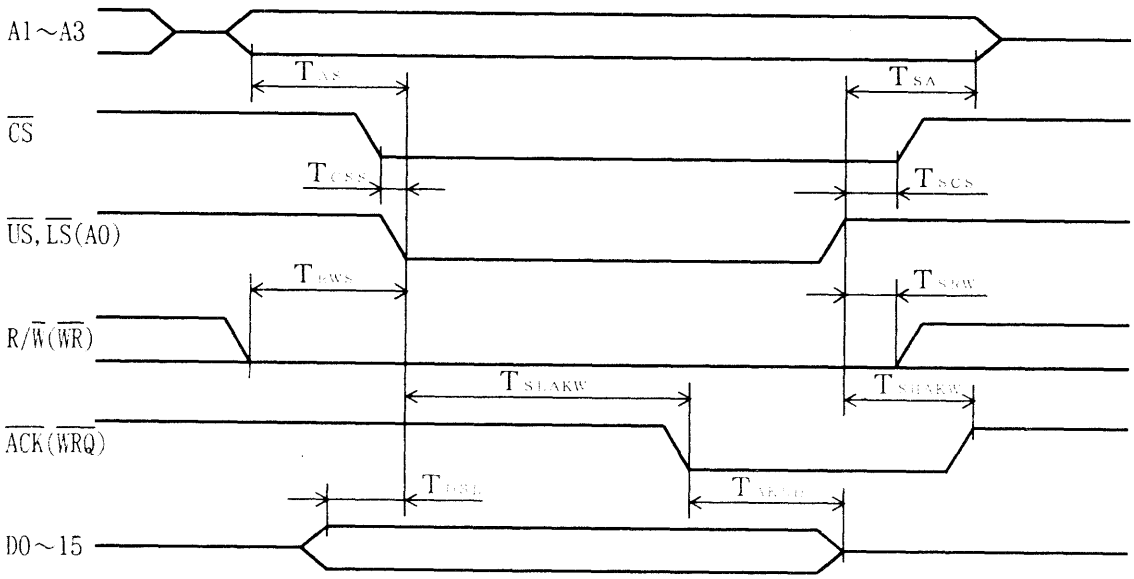
7.4.2 CPU Interface 1 (I/$\overline{M}$=L, B/$\overline{W}$=L) to 68000

Item		Symbol	Condition	Min.	Max.	Unit
Address Setup Time	to $\overline{US}$, $\overline{LS}$ ↓	T_{AS}		23		ns
Address Hold Time	to $\overline{US}$, $\overline{LS}$ ↑	T_{SA}		0		ns
CS Setup Time	to $\overline{US}$, $\overline{LS}$ ↓	T_{CSS}		10		ns
CS Hold Time	to $\overline{US}$, $\overline{LS}$ ↑	T_{SCS}		0		ns
R/$\overline{W}$ Setup Time	to $\overline{US}$, $\overline{LS}$ ↓	T_{RWS}		11		ns
R/$\overline{W}$ Hold Time	to $\overline{US}$, $\overline{LS}$ ↑	T_{SRW}		8		ns
$\overline{ACK}$ ON Delay Time	to $\overline{US}$, $\overline{LS}$ ↓	T_{SLAKR}	C_L=85pF		5·T_{CLK}+45	ns
		T_{SLAKW}	C_L=85pF		6·T_{CLK}+48	ns
$\overline{ACK}$ OFF Delay Time	to $\overline{US}$, $\overline{LS}$ ↑	T_{SHAKR}	C_L=85pF		28	ns
		T_{SHAKW}	C_L=85pF		28	ns
Data Output Advancing Time	to $\overline{ACK}$ ↓	T_{DAKLR}	C_L=85pF	T_{CLK} − 10		ns
Data Float Delay Time	to $\overline{US}$, $\overline{LS}$ ↑	T_{SHD}	C_L=85pF		27	ns
Data Setup Time	to $\overline{US}$, $\overline{LS}$ ↓	T_{DSL}		22		ns
Data Hold Time	to $\overline{ACK}$ ↓	T_{AKDH}		0		ns

Read Cycle



Write Cycle

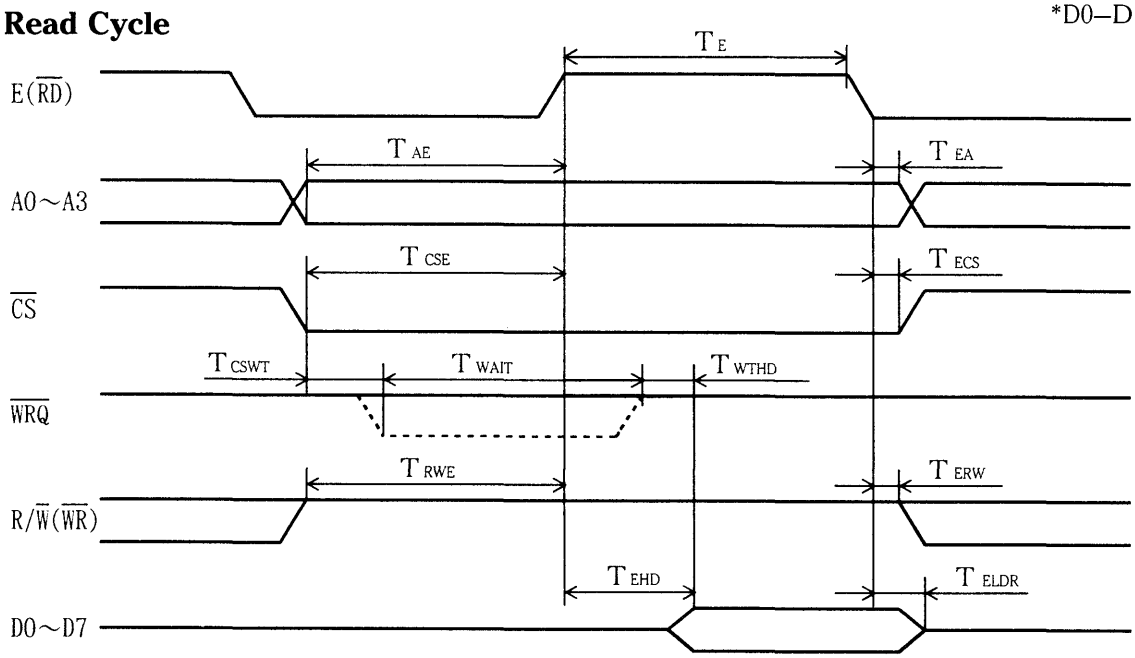


7.4.3 CPU Interface 2 (I/$\overline{M}$=L, B/$\overline{W}$=H) to 6809

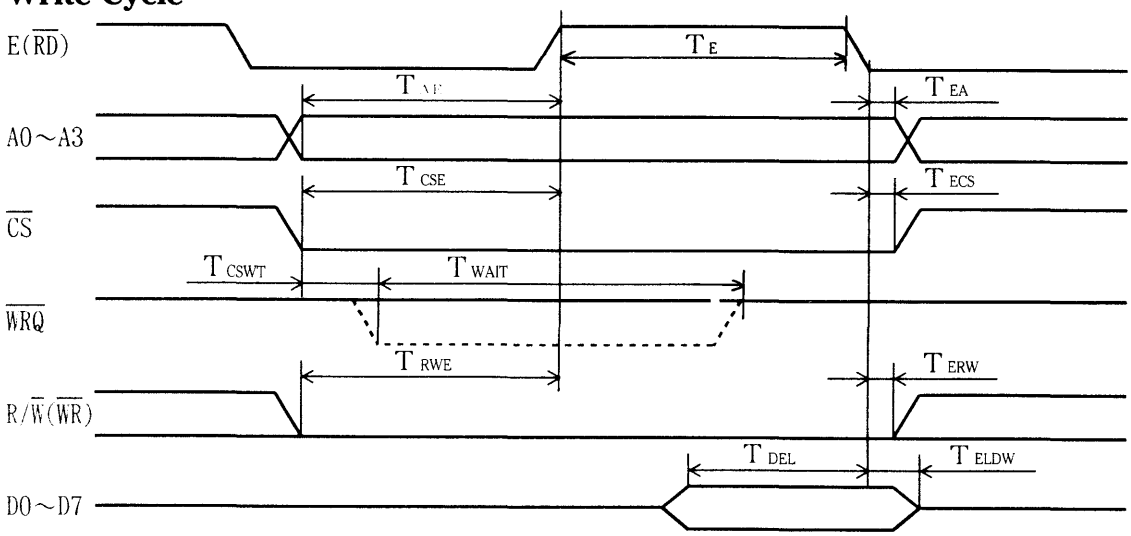
Item		Symbol	Condition	Min.	Max.	Unit
Time Length of E Signal at High Level		T_E	C_L*=85pF	44		ns
Address Setup Time	to E ↑	T_{AE}		23		ns
Address Hold Time	to E ↓	T_{EA}		0		ns
$\overline{CS}$ Setup Time	to E ↑	T_{CSE}		10		ns
$\overline{CS}$ Hold Time	to E ↓	T_{ECS}		0		ns
$\overline{WRQ}$ ON Delay Time	to $\overline{CS}$ ↓	T_{CSWT}	C_L=85pF	46		ns
Time Length of $\overline{WRQ}$ Signal at Low Level		T_{WAIT}			4·T_{CLK}	ns
R/$\overline{W}$ Setup Time	to E ↑	T_{RWE}		11		ns
R/$\overline{W}$ Hold Time	to E ↓	T_{ERW}		8		ns
Data Output Delay Time	to E ↑	T_{EHD}	C_L=85pF		44	ns
Data Output Delay Time	to $\overline{WRQ}$ ↑	T_{WTHD}	C_L=85pF		14	ns
Data Float Delay Time	to E ↓	T_{ELDR}	C_L=85pF		33	ns
Data Setup Time	to E ↑	T_{DEL}		22		ns
Data Hold Time	to E ↓	T_{ELDW}		0		ns

*D0–D7

Read Cycle



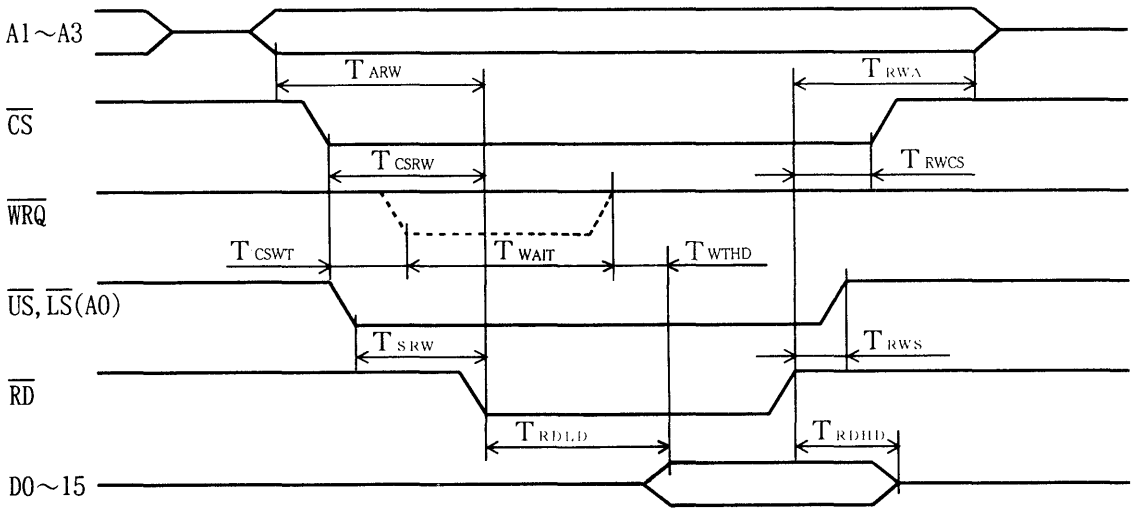
Write Cycle



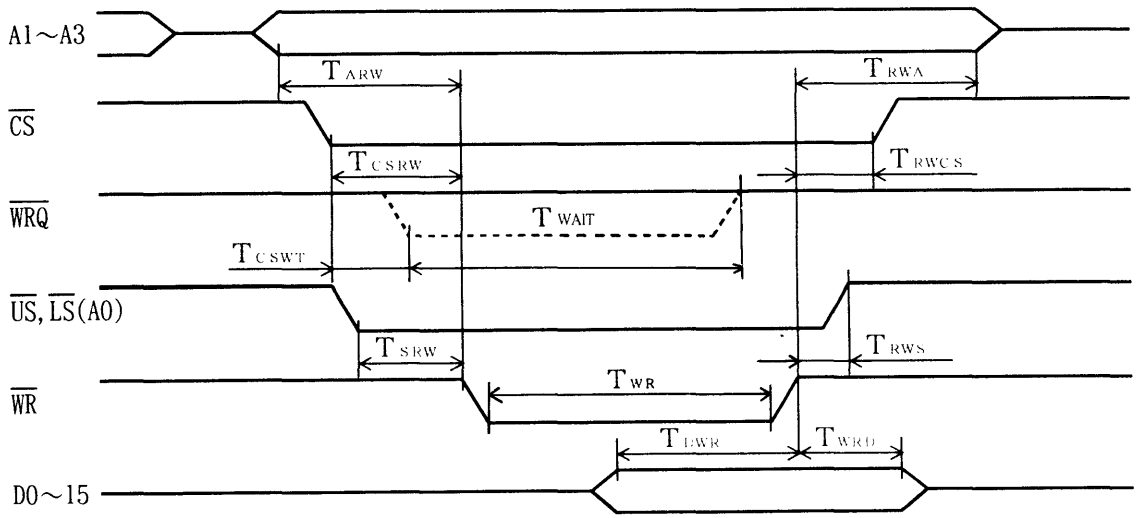
7.4.4 CPU Interface 3 (I/$\overline{M}$=H, B/$\overline{W}$=L) to 8086

Item		Symbol	Condition	Min.	Max.	Unit
Address Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{ARW}		23		ns
Address Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWA}		0		ns
$\overline{CS}$ Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{CSRW}		10		ns
$\overline{CS}$ Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWCS}		0		ns
$\overline{WRQ}$ ON Delay Time	to $\overline{CS}$ ↓	T_{CSWT}	C_L=85pF		46	ns
Time Length of $\overline{WRQ}$ Signal at Low Level		T_{WAIT}			4·T_{CLK}	ns
$\overline{US}$, $\overline{LS}$ Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{SRW}		9		ns
$\overline{US}$, $\overline{LS}$ Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWS}		0		ns
Data Output Delay Time	to $\overline{RD}$ ↓	T_{RDLD}	C_L=85pF		50	ns
Data Output Delay Time	to $\overline{WRQ}$ ↑	T_{WTHD}	C_L=85pF		14	ns
Data Float Delay Time	to $\overline{RD}$ ↑	T_{RDHD}	C_L=85pF		29	ns
$\overline{WR}$ Signal Width		T_{WR}		29		ns
Data Setup Time	to $\overline{WR}$ ↓	T_{DWR}		22		ns
Data Hold Time	to $\overline{WR}$ ↑	T_{WRD}		0		ns

Read Cycle



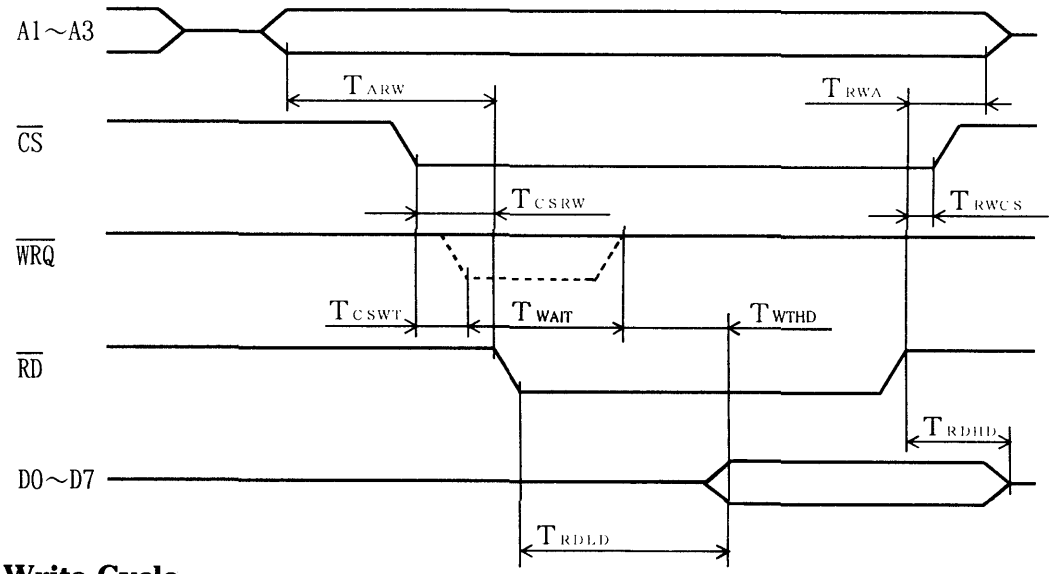
Write Cycle



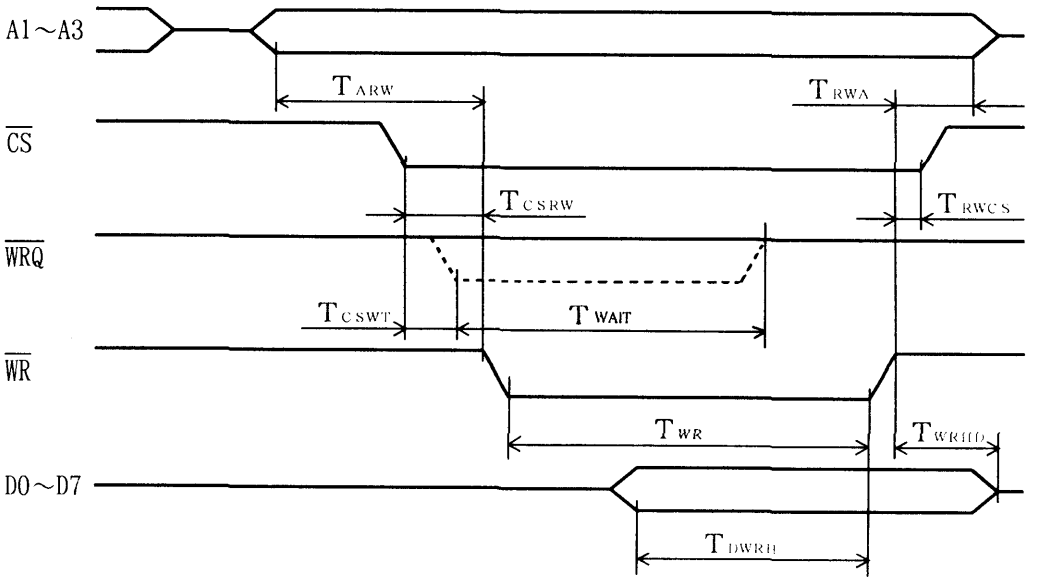
7.4.5 CPU Interface 4 (I/$\overline{M}$=H, B/$\overline{W}$=H) to Z80

Item		Symbol	Condition	Min.	Max.	Unit
Address Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{ARW}		23		ns
Address Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWA}		0		ns
$\overline{CS}$ Setup Time	to $\overline{RD}$, $\overline{WR}$ ↓	T_{CSRW}		10		ns
$\overline{CS}$ Hold Time	to $\overline{RD}$, $\overline{WR}$ ↑	T_{RWCS}		0		ns
$\overline{WRQ}$ ON Delay Time	to $\overline{CS}$ ↓	T_{CSWT}	C_L=85pF		46	ns
Time Length of $\overline{WRQ}$ Signal at Low Level		T_{WAIT}			4·T_{CLK}	ns
Data Output Delay Time	to $\overline{RD}$ ↓	T_{RDLD}	C_L=85pF		50	ns
Data Output Delay Time	to $\overline{WRQ}$ ↑	T_{WTHD}	C_L=85pF		14	ns
Data Float Delay Time	to $\overline{RD}$ ↑	T_{RDHD}	C_L=85pF		33	ns
$\overline{WR}$ Signal Width		T_{WR}		29		ns
Data Setup Time	to $\overline{WR}$ ↑	T_{DWRH}		22		ns
Data Hold Time	to $\overline{WR}$ ↑	T_{WRHD}		0		ns

Read Cycle



Write Cycle

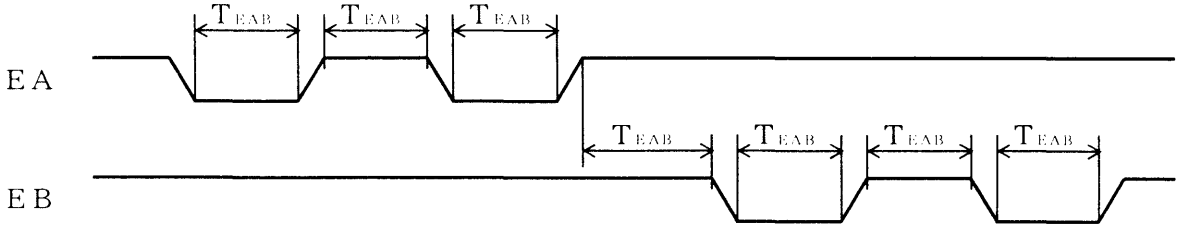


7.4.6 Operation Timing

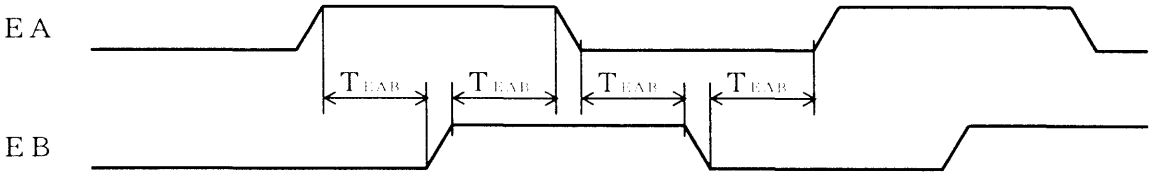
Item	Symbol	Condition	Min.	Max.	Unit
Time Width of Input $\overline{RST}$ Signal		Note 1	8·T_{CLK}		ns
Time Width of Input $\overline{CLR}$ Signal			2·T_{CLK}		ns
Time Width of Input EA and EB Signals	T_{EAB}		2·T_{CLK}		ns
Time Width of Input $\overline{EZ}$ Signal			2·T_{CLK}		ns
Time Width of Input PA and PB Signals	T_{PAB}		2·T_{CLK}		ns
Time Width of Input ERA and ERB Signals	T_{ERAB}		2·T_{CLK}		ns
Time Width of Input $\overline{ALM}$ Signal		Note 2	64·T_{CLK}		ns
Time Width of Input $\overline{INP}$ Signal		Note 2	64·T_{CLK}		ns
Time Width of Input $\overline{ERC}$ Signal			4096·T_{CLK}		ns
Time Width of Input $\overline{\pm EL}$ Signals		Note 2	64·T_{CLK}		ns
Time Width of Input $\overline{\pm SD}$ Signals		Note 2	64·T_{CLK}		ns
Time Width of Input $\overline{ORG}$ Signal		Note 2	64·T_{CLK}		ns
Time Width of Output $\overline{STA}$ and $\overline{STP}$ Signals			512·T_{CLK}		ns
Time Width of Input $\overline{STA}$ and $\overline{STP}$ Signals			8·T_{CLK}		ns
$\overline{BSY}$ Signal ON Delay Time	T_{CMDBSY}		5·T_{CLK}	7·T_{CLK}	ns
	T_{STABSY}		11·T_{CLK}	13·T_{CLK}	ns
Start Delay Time	T_{CMDPLS}		21·T_{CLK}	23·T_{CLK}	ns
	T_{STAPLS}		27·T_{CLK}	29·T_{CLK}	ns
$\overline{OUT}$ Signal ON Delay Time	$T_{ON\ OUT}$	C_L=85pF		55	ns
$\overline{OUT}$ Signal OFF Delay Time	$T_{OF\ OUT}$	C_L=85pF		36	ns
DIR Signal HL Delay Time	$T_{HL\ DIR}$	C_L=85pF		66	ns
DIR Signal LH Delay Time	$T_{LH\ DIR}$	C_L=85pF		44	ns
$\overline{BSY}$ Signal ON Delay Time	$T_{ON\ BSY}$	C_L=85pF		42	ns
$\overline{BSY}$ Signal OFF Delay Time	$T_{OF\ BSY}$	C_L=85pF		34	ns
$\overline{FUP}$ Signal ON Delay Time	$T_{ON\ FUP}$	C_L=85pF		47	ns
$\overline{FUP}$ Signal OFF Delay Time	$T_{OF\ FUP}$	C_L=85pF		34	ns
$\overline{FWD}$ Signal ON Delay Time	$T_{ON\ FDW}$	C_L=85pF		45	ns
$\overline{FDW}$ Signal OFF Delay Time	$T_{OF\ FDW}$	C_L=85pF		34	ns
$\overline{CMP}$ Signal ON Delay Time	$T_{ON\ CMP}$	C_L=85pF		41	ns
$\overline{CMP}$ Signal OFF Delay Time	$T_{OF\ CMP}$	C_L=85pF		28	ns
$\overline{STA}$ Signal ON Delay Time	$T_{ON\ STA}$	C_L=85pF		29	ns
$\overline{STA}$ Signal OFF Delay Time	$T_{OF\ STA}$	C_L=85pF		21	ns
$\overline{STP}$ Signal ON Delay Time	$T_{ON\ STP}$	C_L=85pF		32	ns
$\overline{STP}$ Signal OFF Delay Time	$T_{OF\ STP}$	C_L=85pF		21	ns
$\overline{ERC}$ Signal ON Delay Time	$T_{ON\ ERC}$	C_L=85pF		66	ns
$\overline{ERC}$ Signal OFF Delay Time	$T_{OF\ ERC}$	C_L=85pF		26	ns
$\overline{INT}$ Signal ON Delay Time 1	$T_{ON\ IT1}$	C_L=85pF*3		65	ns
$\overline{INT}$ Signal ON Delay Time 2	$T_{ON\ IT2}$	C_L=85pF*4		34	ns
$\overline{INT}$ Signal OFF Delay Time	$T_{OF\ INT}$	C_L=85pF		34	ns

NOTES: 1. Eight cycles of CLK signal should be input during the time the $\overline{RST}$ pin is at low level.
2. Setting bit 8 of R6 at 1 makes a minimum time 2·T_{CLK}.
3. In the case the $\overline{INT}$ signal is output due to a cause other than a signal input to AP0, AP1 or AP2.
4. In the case the $\overline{INT}$ signal is output due to a signal input to AP0, AP1 or AP2.

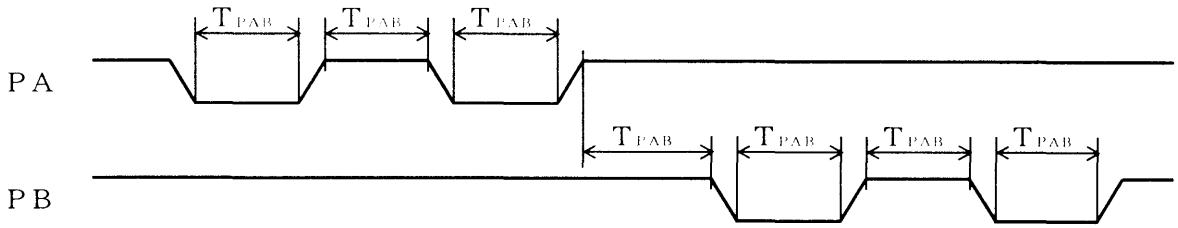
(1) EA and EB Input in 2-pulse Mode



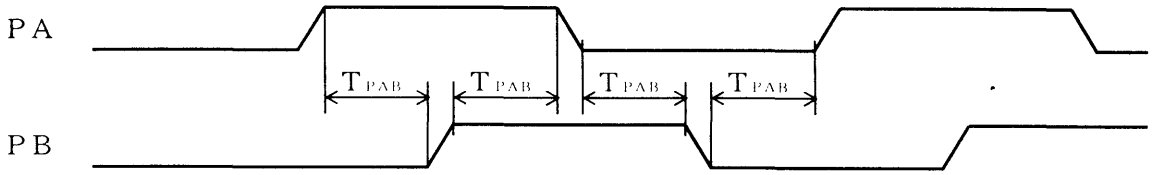
(2) EA and EB Input in 90° Phase Difference Mode



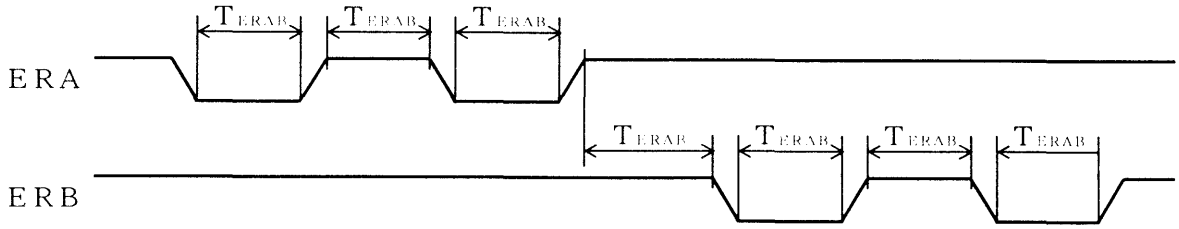
(3) PA and PB Input in 2-pulse Mode



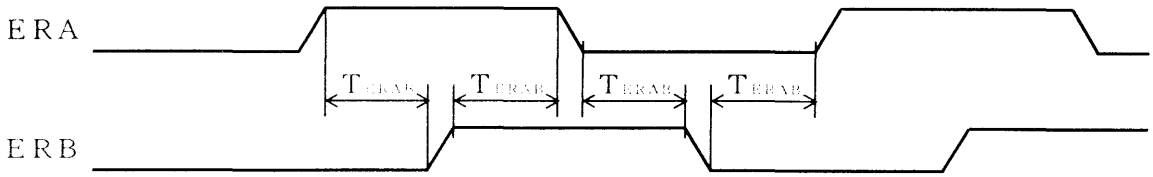
(4) PA and PB Input in 90° Phase Difference Mode



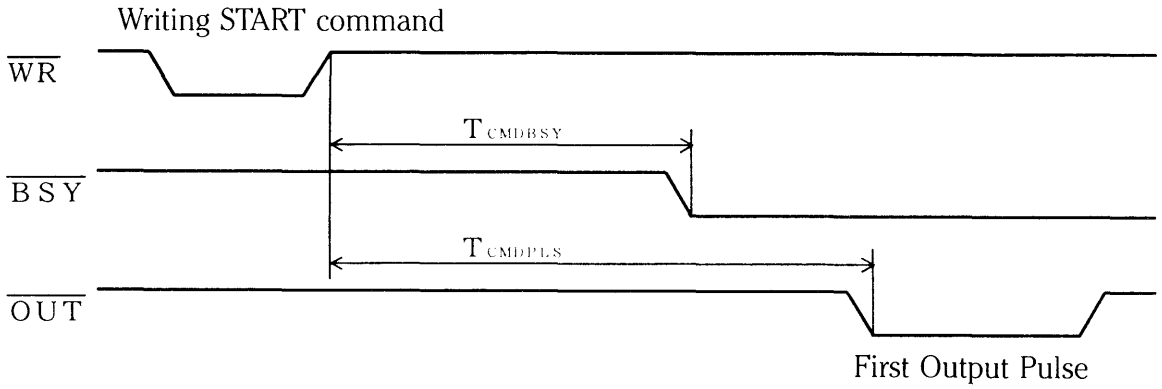
(5) ERA and ERB Input in 2-pulse Mode



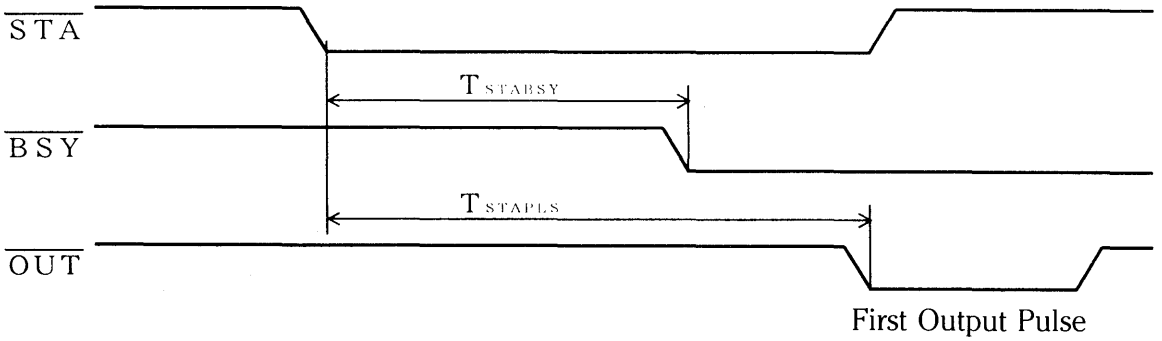
(6) ERA and ERB Input in 90° Phase Difference Mode



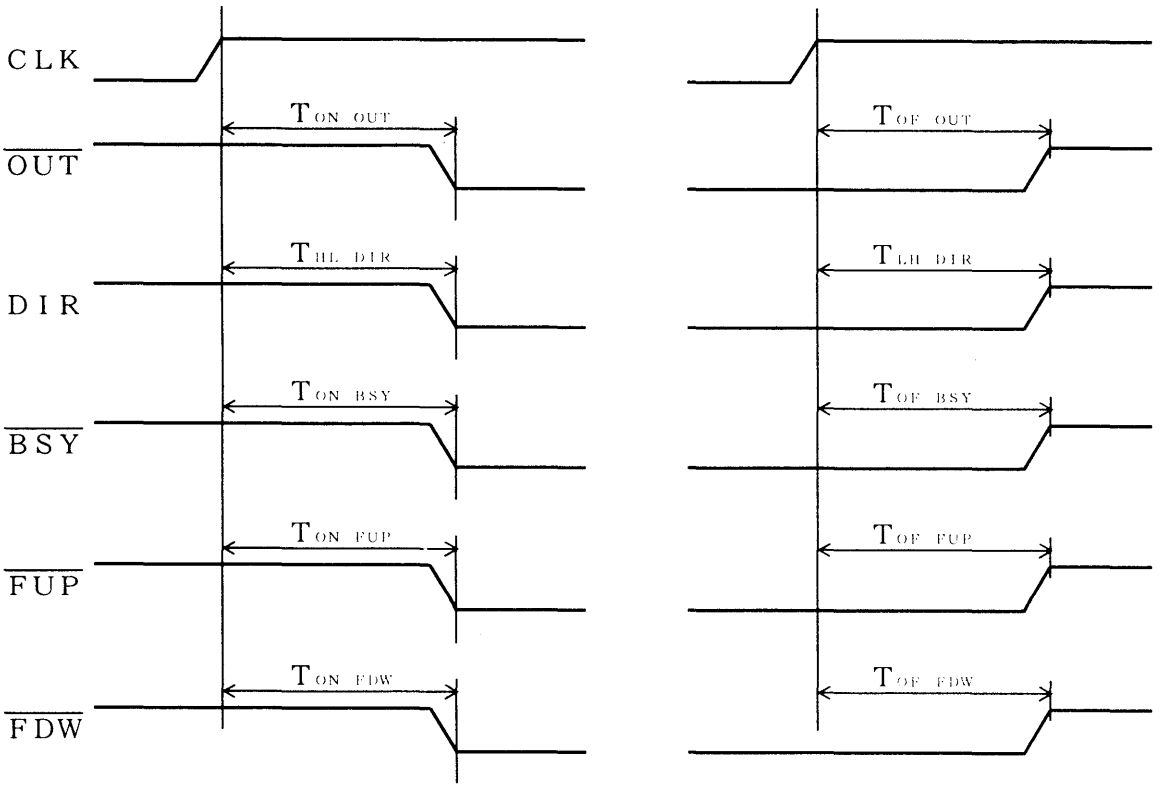
(7) Command Start Timing with I/$\overline{M}$=H and B/$\overline{W}$=H

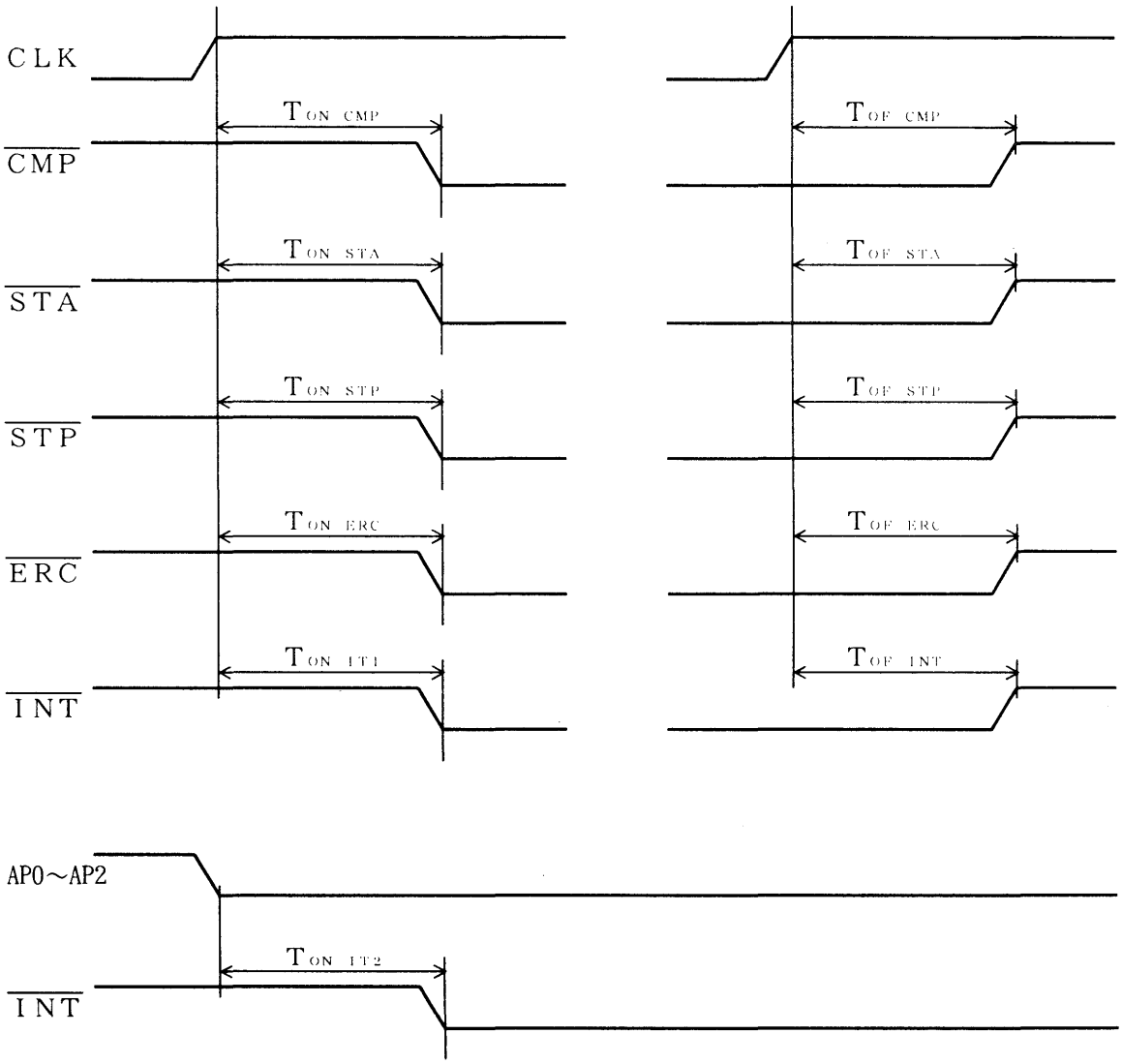


(8) Simultaneous Start Timing



(9) OUT Signal Delay Time




CLK
$T_{ON\ CMP}$
$\overline{CMP}$
$T_{ON\ STA}$
$\overline{STA}$
$T_{ON\ STP}$
$\overline{STP}$
$T_{ON\ ERC}$
$\overline{ERC}$
$T_{ON\ IT1}$
$\overline{INT}$
$T_{OF\ CMP}$
$T_{OF\ STA}$
$T_{OF\ STP}$
$T_{OF\ ERC}$
$T_{OF\ INT}$

AP0～AP2
$T_{ON\ IT2}$
$\overline{INT}$

8. Handling Precautions

8.1 Designing Precautions

(1) In any case the PCL5014 shall not be subjected to a condition exceeding the absolute maximum ratings.

(2) Protect the PCL5014 from receiving a heating effect from environment and keep ambient temperatures as lowest possible.

(3) A latch-up condition may cause heat generation and fuming. Take the following precautions:

- Do not make the voltage level of input/output pins higher than Vdd and lower than GND. Also, take the power-up timing into consideration.
- Do not apply abnormal noise to the PCL5014.
- Fix the potential of unused input/output pins to Vdd or GND.
- Do not short-circuit the output.
- Protect the PCL5014 against induction and static electricity from a high-voltage generation circuit.

(4) Take care that an excess voltage due to noise, surge and static electricity is not applied to the PCL5014.

8.2 Transportation and Storage Precautions

(1) Handle the packaging gently. Throwing or dropping it may damage the PCL5014 in it.

(2) Do not store the packaging where it may be splashed with water or exposed to direct sunlight.

(3) Do not store the packaging where poisonous or corrosive gases are generated.

(4) Prepare an anti-static container and take care that the PCL5014 may not receive any load.

8.3 Assembling Precautions

(1) Take the following precautions to protect the PCL5014 against damage due to static electricity:

- Ground the instruments and fixtures which are installed at the assembling area.
- Ground the worktable with a conductive mat or the like having resistance. Avoid the metal surface which causes an abrupt electrical discharge with low resistance if an electrified PCL5014 contacts with the surface.
- When picking up the PCL5014 with vacuum, mount a conductive rubber or the like onto the tip of pickup to prevent the PCL5014 from being electrified. Also, use contacts featuring highest possible resistance for connection to lead terminals of PCL5014.

- Tweezers which may contact with pins of PCL5014 should be resistant against static electricity. Avoid metal tweezers if possible. Such tweezers may electrify the PCL5014 through friction and cause electrical discharge.

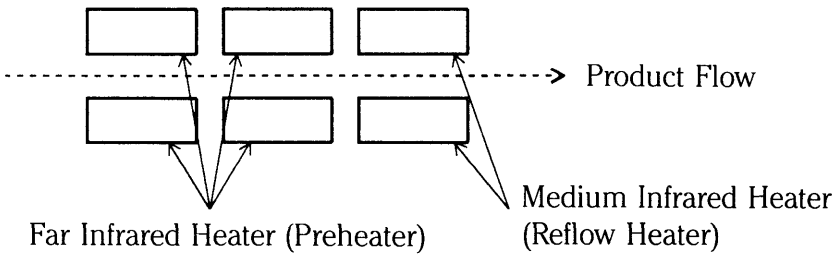
(2) The worker should wear a wrist strap, which should be grounded via 1MΩ resistor.

(3) Use a low-voltage soldering iron and ground it at the tip.

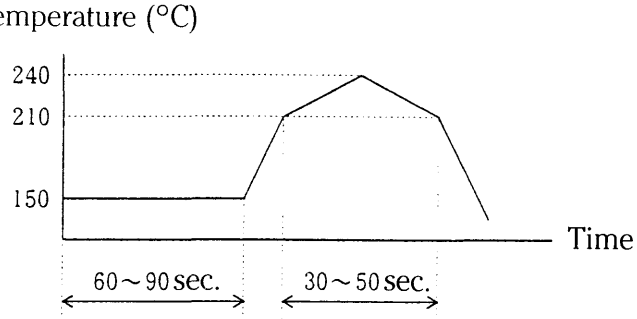
(4) Do not place the PCL5014 or the container near instruments, such as CRT, which generate a high electrical field.

(5) If the fully heating soldering method is used, conduct high-temperature dehumidifying treatment at 125°C for 20 hours.

(6) If soldering is made through an infrared reflow method for reduction of heat stress, the far and medium infrared reflow method is recommended.

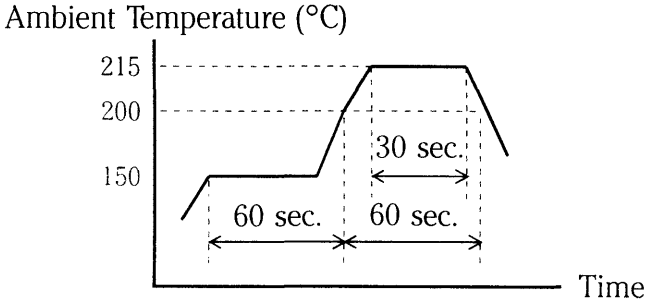


Soldering should be done in such a manner that the time length the package surface and PC board surface are heated to a range of 210°C to 240°C maximum is less than 30 seconds.



(7) For the warm-air reflow, use the same procedure as the far infrared method.

(8) For the vapor phase soldering, Florinade FC-704 or the equivalent is recommended as the solution. Time lengths of heating should be within 30 seconds at 215°C and within 60 seconds at 200°C.



(9) In the case of soldering iron, soldering should be done within 10 seconds at maximum 260°C or within 3 seconds at maximum 350°C.

8.4 Other Precautions

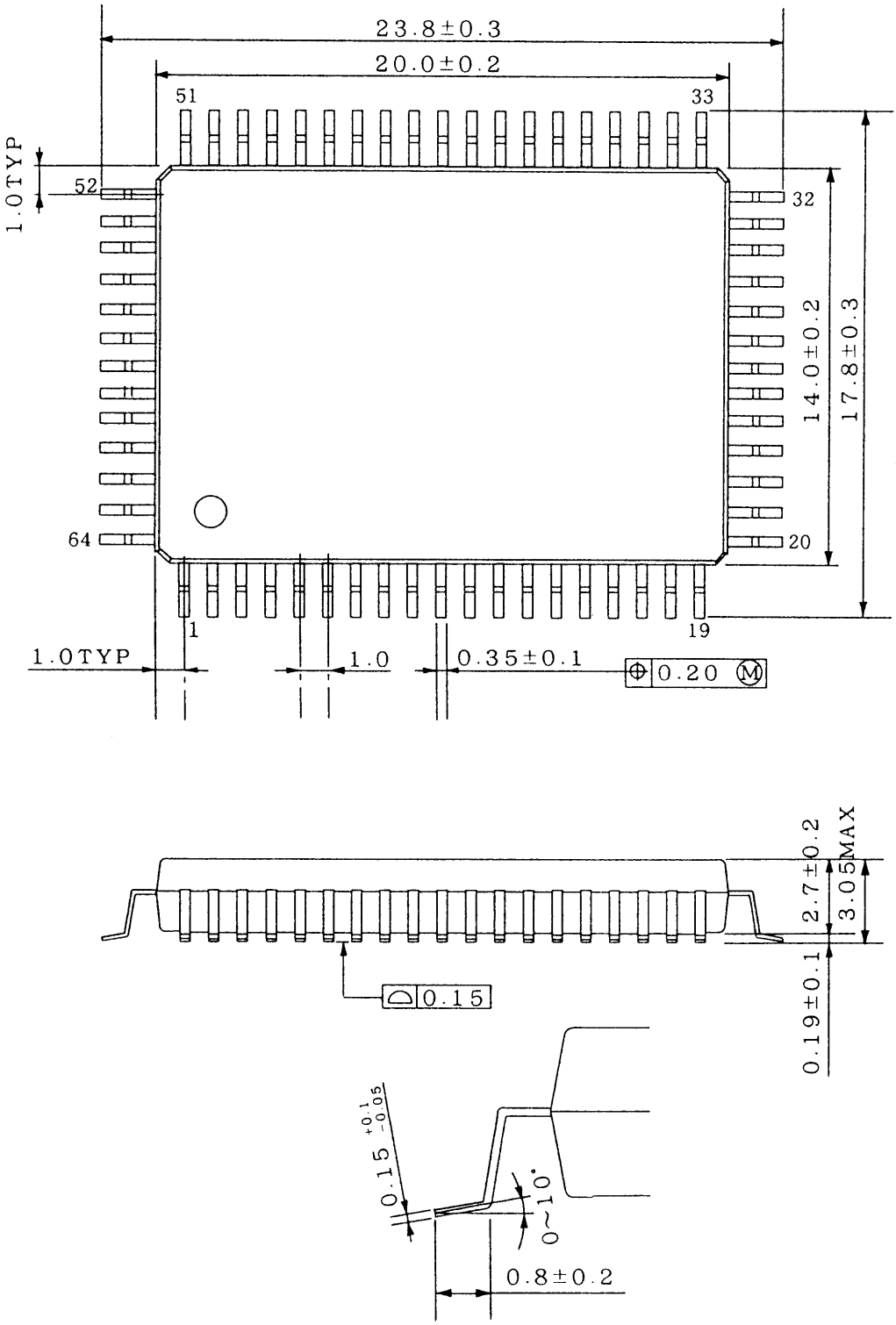
(1) If the PCL5014 is intended for use under adverse environmental conditions (humidity, corrosive gases or dirt), take proper measures such as humidity-resistant coating.

(2) Resin materials used for the package are flame-retardant but not non-inflammable. So it may be burned or fume. Avoid placing it near an inflammable material.

(3) The PCL5014 is designed for office appliances, communications equipment, measuring instruments and home electric appliances. If you use it for the system of which a trouble or erroneous operation may lead to the death or injure the operator, such as nuclear control system, space ship, traffic signal, combustion control system or safety device, take sufficient care.

9. External Dimensions

Unit: mm



10. Appendix

10.1 List of Commands

10.1.1 Start Commands

Command	Description
10HEX	Start constant-speed operation at FL rate.
11HEX	Start constant-speed operation at FH rate.
13HEX	Start varied-speed operation.
14HEX	Start suspended constant-speed operation at FL rate.
15HEX	Start suspended constant-speed operation at FH rate.
17HEX	Start suspended varied-speed operation.
30HEX	Start plural units of PCL5014 outputting pulses simultaneously.

10.1.2 Speed Change Commands

Command	Description
00HEX	Change the pulse rate to FL rate instantaneously.
01HEX	Change the pulse rate to FH rate instantaneously.
02HEX	Ramp down the pulse rate to FL rate.
03HEX	Ramp up the pulse rate to FH rate.

10.1.3 Stop Commands

Command	Description
09HEX	Stop the PCL5014 from generating pulses immediately.
0AHEX	Initiate deceleration then stop the PCL5014 from generating pulses.
28HEX	Stop plural units of PCL5014 from generating pulses simultaneously.

10.1.4 Start Retention Commands

Command	Description
20HEX	Retain the start of constant-speed operation at FL rate.
21HEX	Retain the start of constant-speed operation at FH rate.
23HEX	Retain the start of varied-spped operation.
24HEX	Retain the start of suspended constant-speed operation at FL rate.
25HEX	Retain the start of suspended constant-speed operation at FH rate.
27HEX	Retain the start of suspended varied-speed operation.

10.1.5 General-Purpose I/O Setting Commands

Command	Description
40HEX	Reset BP0 general-purpose output pin to low level.
41HEX	Reset BP1 general-purpose output pin to low level.
42HEX	Reset BP2 general-purpose output pin to low level.
43HEX	Reset BP3 general-purpose output pin to low level.
44HEX	Reset BP4 general-purpose output pin to low level.
45HEX	Reset BP5 general-purpose output pin to low level.
46HEX	Reset BP6 general-purpose output pin to low level.
47HEX	Reset BP7 general-purpose output pin to low level.
48HEX	Reset AP0 general-purpose output pin to low level.
49HEX	Reset AP1 general-purpose output pin to low level.
4AHEX	Reset AP2 general-purpose output pin to low level.
50HEX	Set BP0 general-purpose output pin to high level.
51HEX	Set BP1 general-purpose output pin to high level.
52HEX	Set BP2 general-purpose output pin to high level.
53HEX	Set BP3 general-purpose output pin to high level.
54HEX	Set BP4 general-purpose output pin to high level.
55HEX	Set BP5 general-purpose output pin to high level.
56HEX	Set BP6 general-purpose output pin to high level.
57HEX	Set BP7 general-purpose output pin to high level.
58HEX	Set AP0 general-purpose output pin to high level.
59HEX	Set AP1 general-purpose output pin to high level.
5AHEX	Set AP2 general-purpose output pin to high level.

10.1.6 Control Commands

Command	Description
60HEX	Reset programmed settings.
61HEX	Reset the up/down counter.
62HEX	Reset the deviation counter for out-of-step detection.
63HEX	Emergency stop
64HEX	Reset the output $\overline{\text{ERC}}$ signal.
65HEX	Reset the output $\overline{\text{STA}}$ or $\overline{\text{STP}}$ signal.
66HEX	Settle preregisters.
67HEX	Unsettle preregisters.

10.1.7 Register Read/Write Commands

Command	Description
80HEX	Read the parameter from the R0 register.
81HEX	Read the parameter from the R1 register.
82HEX	Read the parameter from the R2 register.
83HEX	Read the parameter from the R3 register.
84HEX	Read the parameter from the R4 register.
85HEX	Read the parameter from the R5 register.
86HEX	Read the parameter from the R6 register.
87HEX	Read the parameter from the R7 register.
88HEX	Read the parameter from the R8 register.
89HEX	Read the parameter from the R9 register.
8AHEX	Read the parameter from the R10 register.
8BHEX	Read the parameter from the R11 register.
8CHEX	Read the parameter from the R12 register.
8DHEX	Read the parameter from the R13 register.
8EHEX	Read the parameter from the R14 register.
90HEX	Read the parameter from the R0 preregister.
91HEX	Read the parameter from the R1 preregister.
92HEX	Read the parameter from the R2 preregister.
93HEX	Read the parameter from the R3 preregister.
94HEX	Read the parameter from the R4 preregister.
95HEX	Read the preset counter value.
96HEX	Read the ramping-down point counter value.
97HEX	Read the parameter from the R5 preregister.
98HEX	Read the parameter from the R15 preregister.
99HEX	Read the parameter from the R16 preregister.
9AHEX	Read the parameter from the R15 register.
9BHEX	Read the parameter from the R16 register.
C0HEX	Write the parameter in the R0 preregister.
C1HEX	Write the parameter in the R1 preregister.
C2HEX	Write the parameter in the R2 preregister.
C3HEX	Write the parameter in the R3 preregister.
C4HEX	Write the parameter in the R4 preregister.
C5HEX	Write the parameter in the R5 preregister.
C6HEX	Write the parameter in the R6 register.
C7HEX	Write the parameter in the R7 register.
C8HEX	Write the parameter in the R8 register.
C9HEX	Write the parameter in the R9 register.

10.1.7 Register Read/Write Commands, continued

Command	Description
CA$_{HEX}$	Write the parameter in the R10 register.
CB$_{HEX}$	Write the parameter in the R11 register.
D1$_{HEX}$	Write the parameter in the R1 register.
D2$_{HEX}$	Write the parameter in the R2 register.
D3$_{HEX}$	Write the parameter in the R3 register.
D7$_{HEX}$	Write the parameter in the R5 register.
D8$_{HEX}$	Write the parameter in the R15 preregister.
D9$_{HEX}$	Write the parameter in the R16 preregister.
DA$_{HEX}$	Write the parameter in R15 register.
DB$_{HEX}$	Write the parameter in R16 register.

10.2 Codes for Interrupt Signal Generating Factors

Code	Factor
00$_{HEX}$	$\overline{INT}$ output is in OFF status.
01$_{HEX}$	Deceleration-stop command (0A$_{HEX}$) stops pulse output after deceleration.
02$_{HEX}$	In-positioning stops the PCL3013 from outputting pulses.
03$_{HEX}$	Origin return (origin search) stops the PCL3013 from outputting pulses.
04$_{HEX}$	Origin escape stops the PCL3013 from outputting pulses.
05$_{HEX}$	Immediate stop command (09$_{HEX}$) stops the PCL3013 from outputting pulses.
06$_{HEX}$	$\overline{STP}$ signal stops the PCL3013 from outputting pulses.
07$_{HEX}$	$\overline{-EL}$ signal stops the PCL3013 from generating pulses.
08$_{HEX}$	$\overline{+EL}$ signal stops the PCL3013 from generating pulses.
09$_{HEX}$	$\overline{-SD}$ signal stops the PCL3013 from generating pulses.
0A$_{HEX}$	$\overline{+SD}$ signal stops the PCL3013 from generating pulses.
0B$_{HEX}$	$\overline{ALM}$ signal stops the PCL3013 from generating pulses.
0C$_{HEX}$	Out-of-step detection stops the PCL3013 from generating pulses.
0D$_{HEX}$	AP0 pin changes from high to low level.
0E$_{HEX}$	AP1 pin changes from high to low level.
0F$_{HEX}$	AP2 pin changes from high to low level.
10$_{HEX}$	$\overline{CLR}$ signal resets the present position counter.
11$_{HEX}$	EA and EB signal input error
12$_{HEX}$	PA and PB signal input error
13$_{HEX}$	ERA and ERB signal input error
14$_{HEX}$	Start of the next operation (parameters in preregisters can be revised)
15$_{HEX}$	The PCL3013 starts deceleration.
16$_{HEX}$	Comparate condition changes from false to true.

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